Linear and Interface Circuit Applications

Volume 1

Amplifiers, Comparators, Timers, and Voltage Regulators

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TEXAS INSTRUMENTS

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Section 1

Introduction

The technology of incorporating microprocessors and other logic circuits in single integrated circuit chips has heralded the computer age. Linear and interface circuits have also been developed to provide the variety of functions required for computer devices to interface with each other and external systems. The broad range of integrated circuits available today can therefore be divided into two general classes: logic and linear.

This is the first in a new series of application books that address the linear devices. The books have been divided into basically independent sections for ease of use. Each section covers a product category, beginning with the basic theory, followed by the key characteristics of devices in that category and then applications of the devices.

The objective of this book is to assist the user in understanding the operating principles and characteristics of the wide variety of linear devices. By a better understanding of the devices the user can solve the common application problem of selecting the most suitable device for a particular application. Emphasis is placed on demonstrating operating characteristics and their potential uses in circuits. Obviously presentation of all possible circuits is beyond the scope of any book. The circuit examples selected for this book have accrued from customer enquiries and related laboratory simulations. In many cases they are solutions to actual customer design problems. The circuits are presented as examples to stimulate the readers thinking on how the devices could be used to solve specific design requirements. A data sheet should be referred to for complete device characteristics and operating limits.

This volume 1 discusses operational amplifiers, comparators, video amplifiers, voltage references and timers. Volume 2 will present information on display drivers and data line drivers, receivers and transceivers. Volume 3 will provide information on peripheral drivers, data acquisition circuits and special functions.

Table 1–1   Linear and Interface Circuits.

XXX XXXXX XX

└── Package Type
(See Table 1-2)

ORIGINAL MANUFACTURER	TI PREFIX	DEVICE NUMBER	TEMP* RANGE
TI	TL or TLC	XXXC	COM
		XXXI	IND/AUTO
		XXXM	MIL
	SN	75XXX	COM
		55XXX	MIL
NATIONAL	LM	1XXX	MIL
		2XXX	IND
		3XXX	COM
	ADC	XXXX	COM
	DS	78XX	MIL
		88XX	COM
RAYTHEON	RC	4XXX	COM
	RM	4XXX	MIL
SIGNETICS	NE	5/55XX	COM
	SA	5/55XX	AUTO
	SE	5/55XX	MIL
	N8T	XX	COM
FAIRCHILD	uA	7XXXC	COM
		7XXXI	IND
		7XXXM	MIL
	uA	9XXX	COM
MOTOROLA	MC	13/33XX	IND
		14/34XXX	COM
		15/35XX	MIL
SPRAGUE	UCN	XXX	COM
	UDN	XXXX	COM
	ULN	XXXX	COM
AMD	AM	XXXXXM	MIL
		XXXXXC	COM
SILICON GENERAL	SG	15XX	MIL
		25XX	IND
		35XX	COM
PMI	OP-	XX	COM

*Temperature ranges:

COM = 0 °C to 70 °C	AUTO = −40 °C to 85 °C
IND = −25 °C to 85 °C	MIL = −55 °C to 125 °C

As an overview of the device numbering system, Table 1–1 shows the meaning of the various characters in Texas Instruments Linear and Interface circuit device numbers. Texas Instruments devices that are direct alternate sources for other manufacturers' parts carry the original part number including its prefix. Alterations in device characteristics from the original data sheet specifications, generally to improve performance, results in a new number with the appropriate SN55, SN75, or TL prefix. The type of package is also included in the device number. Table 1–2 lists the package suffixes and their definitions.

Table 1–2   Packages.

TYPE	PACKAGE DESCRIPTION
N	Plastic DIP
NE	Plastic DIP, copper lead frame
NF	Plastic DIP, 28 pin, 400 mil
NT	Plastic DIP, 24 pin, 300 mil
P	Plastic DIP, 8 pin
D	Plastic SO, small outline
J	Ceramic DIP
JD	Ceramic DIP, side braze
JG	Ceramic DIP, 8 pin
FK	Ceramic chip carrier, square
FN	Plastic chip carrier, square
KA	TO-3 metal can
KC	TO-220 plastic, power tab
LP	TO-226 plastic
U	Ceramic flatpack, square
W, WC	Ceramic flatpack, rectangular

Section 2

Operational Amplifier and Comparator Theory

OPERATIONAL AMPLIFIER THEORY

In 1958, the age of the integrated circuit was ushered in by Jack Kilby of Texas Instruments.

From the two hand-built circuits which he fabricated, the variety and quantity of integrated circuits have mushroomed at an ever increasing rate. One type of integrated circuit is the operational amplifier. It has become one of the most widely used integrated circuits because of its versatility and ease of application.

One of the two hand-built integrated circuits which Jack Kilby built was a phase shift oscillator, the first linear integrated circuit. This was soon followed by the introduction of the uA702 and SN523 operational amplifiers. Even with their requirements for complex compensation they quickly gained acceptance. Among the improved designs which quickly followed was the uA741 single operational amplifier which required no external compensation. Conversely, the uA748 was designed for compensation by external components to change the frequency response for applications requiring wider bandwidth and higher slew rate.

Operational amplifier capabilities and versatility are achieved by connecting external components to provide the desired transfer functions.

Typical operational amplifier characteristics include frequency response, signal phase shift, slew rate and gain.

To adequately evaluate the potential of an operational amplifier for a specific application, an understanding of operational amplifier characteristics is required. Figure 2–1 represents an equivalent operational amplifier circuit and its parameters. The parameters illustrated in Figure 2–1 are as follows:

● Input bias currents (I_{IB1} and I_{IB2}) – the current flowing into both operational amplifier inputs. In an ideal condition, I_{IB1} and I_{IB2} are equal.
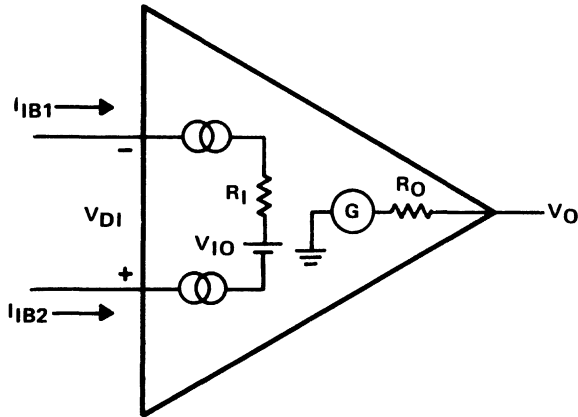
Fig. 2–1   Operational Amplifier Equivalent Circuit.

● Differential input voltage (V_{DI}) – the differential input voltage between the noninverting ($+$) and the inverting ($-$) input.

● Input offset voltage (V_{IO}) – an internally generated input voltage identified as the voltage that must be applied to the input terminals to produce an output of 0 V.

● Input resistance (R_I) – the resistance at either input when the other input is grounded.

● Output voltage (V_O) – normal output voltage as measured to ground.

● Output resistance (R_O) – resistance at the output of the operational amplifier.

● Differential voltage gain (A_{VD}) or open-loop voltage gain (A_{OL}) – the ratio of the input voltage to the output voltage of the operational amplifier without external feedback.

● Bandwidth (BW) – the band of frequencies over which the gain (V_O/V_{DI}) of the operational amplifier remains within desired limits. Usually quoted at unity gain or as gain – bandwidth product.

The generator symbol ⑥ in Figure 2–1 represents the output voltage resulting from the product of the gain and the differential input voltage ($A_{VD} \, V_{DI}$).

An ideal operational amplifier (see Figure 2–2) provides a linear output voltage that is proportional to the difference in voltage between the two input terminals. The output voltage will have the same polarity as that of the noninverting (+) input with respect to the voltage at the inverting (−) input. When the noninverting input is more positive than the inverting input, the output voltage will have a positive amplitude. When the noninverting input is more negative than the inverting input, the output voltage will have a negative amplitude.
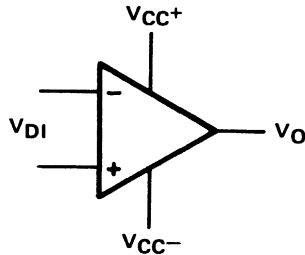
Fig. 2–2   Ideal Operational Amplifier.

An operational amplifier having no external feedback from output to input is described as being in the open-loop mode. In the open-loop mode, the characteristics of the ideal operational amplifier are as follows:

Differential gain $= \rightarrow \infty$

Common-mode gain $= 0$

Input resistance $= \rightarrow \infty$

Output resistance $= 0$

Bandwidth $= \rightarrow \infty$

Offset and drift $= 0$

MAJOR PERFORMANCE CHARACTERISTICS

The detailed and specific performance characteristics of a particular operational amplifier can be found on the appropriate data sheet. The electrical characteristics provided are for a specified supply voltage and ambient temperature and usually will have minimum, typical, and

maximum values. Additional major operational amplifier characteristics and their meaning are as follows:

- Input offset current (I_{IO}) – the difference between the two input bias currents when the output voltage is zero.

- Common-mode input voltage range (V_{ICR}) – the range of the common-mode input voltage (i.e., the voltage common to both inputs).

- Output short-circuit current (I_{OS}) – the maximum output current that the operational amplifier can deliver into a short circuit.

- Output voltage swing (V_{OPP}) – the maximum peak-to-peak output voltage that the operational amplifier can produce without saturation or clipping occurring. This characteristic is dependent upon output load resistance.

- Slew rate (SR) – the time rate of change of the closed-loop output voltage with the operational amplifier circuit having a voltage gain of unity (1).

- Supply current (I_{CC}) – the total current that the operational amplifier will draw from both power supplies when unloaded (per amplifier for multiunit packages).

- Common-mode rejection ratio (CMRR) – a measure of the ability of an operational amplifier to reject signals that are present at both inputs simultaneously. The ratio of the common-mode input voltage to the generated output voltage is usually expressed in decibels (dB).

The preceding paragraphs have discussed basic operational amplifier characteristics. The following paragraphs will provide more detailed information.

Gain, Frequency Response and Gain-Bandwidth Product

Unlike the ideal operational amplifier, a typical operational amplifier has a finite differential gain and bandwidth. The open-loop gain of a TL321 operational amplifier is shown in Figure 2–3. At low frequencies, open-loop gain is constant. At approximately 6 Hz it begins to roll off ultimately at the rate of −6 dB/octave (an octave is a doubling in frequency and decibels are a measure of gain calculated by

$20 \log_{10} V_O/V_I$). The frequency at which the gain reaches unity is called unity gain bandwidth and referred to as B1.
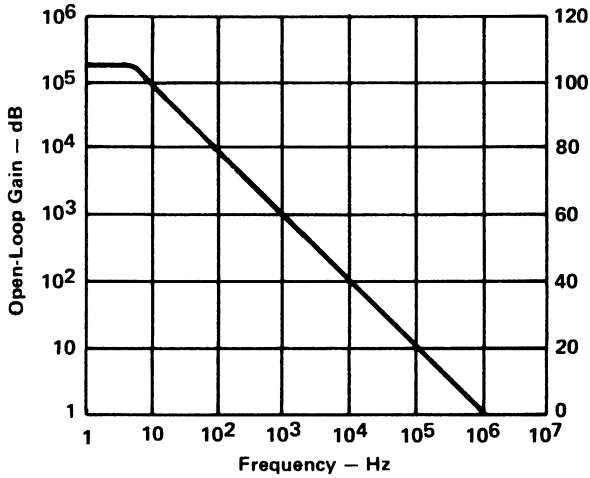
Fig. 2–3   TL321 Operational Amplifier Bandwidth.
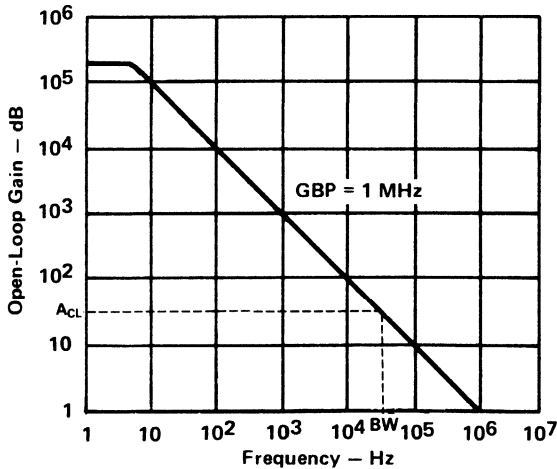
Gain-Bandwidth Product = Closed-Loop Gain X Frequency Response

Fig. 2–4   Bandwidth for Operational Amplifier TL321.

This is also referred to as gain-bandwidth product and when selecting an operational amplifier for a particular application, it is one of the primary factors to consider. The product of closed-loop gain and frequency response (expressed as bandwidth, BW) remains constant at any point on the linear portion of the open-loop gain curve (see Figure 2–4).

The bandwidth is the frequency at which the closed-loop gain A_{CL} curve intersects the open-loop curve as shown in Figure 2–4. The bandwidth may be obtained for any desired closed-loop gain by drawing a horizontal line from the desired gain to the roll-off intersection of the open-loop gain curve. In a typical design, a factor of 1/10 or less of the open loop gain at a given frequency should be used. This ensures that the operational amplifier will function properly with minimum distortion. When the closed loop voltage gain of an operational amplifier circuit is increased, the bandwidth will decrease.

Influence of the Input Resistance

The influence of the input resistance can be determined with Kirchhoff's law. By applying Kirchhoff's law to the circuit in Figure 2–5, we can use the following equations:

$$I_1 = I_2 + I_3 \text{ or}$$

$$\frac{V_I - V_{DI}}{R1} = \frac{V_{DI} - V_O}{R2} + \frac{V_{DI}}{R_I}$$
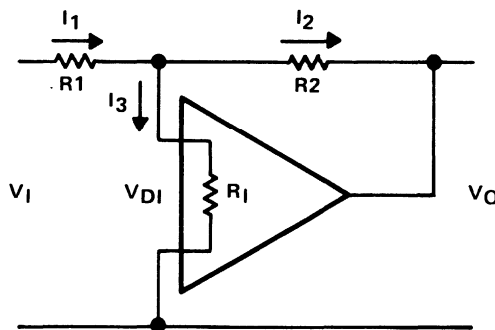
Fig. 2–5   Influence of the Input Resistance.

If the open-loop gain is infinite, the differential input voltage will be zero and the value of input resistance (if it is not zero) will have no influence. Since $V_{DI} = V_O/A_{VD}$, the following equations apply:

$$\frac{V_I - \dfrac{V_O}{A_{VD}}}{R1} = \frac{\dfrac{V_O}{A_{VD}} - V_O}{R2} + \frac{\dfrac{V_O}{A_{VD}}}{R_I}$$

Therefore:

$$\frac{V_I}{V_O} = \frac{1}{A_{VD}} + \frac{1}{\dfrac{R2}{R1} A_{VD}} + \frac{R1}{R_I A_{VD}} - \frac{1}{\dfrac{R2}{R1}}$$

or:

$$\frac{V_I}{V_O} = -\frac{1}{\dfrac{R2}{R1}} + \frac{1}{\dfrac{R2}{R1} A_{VD}} + \frac{1}{A_{VD}} \left(1 + \frac{R1}{R_I} \right)$$

The previous listed equations indicate that the input resistance will have little or no effect on the ratio of output voltage to input voltage for very large values of A_{VD}. Therefore, the closed-loop gain for typical applications is independent of the input resistance.

Influence of Input Offset Voltage

The input offset voltage (V_{IO}) is a differential input voltage resulting from the mismatch of the operational amplifier input stages and may be considered as a voltage inserted between the two inputs.

The effect on currents I_1 and I_2 can be determined by the following equations:

$$\frac{V_I - V_{IO}}{R1} = \frac{V_{IO} - V_O}{R2}$$

If the input voltage (V_I) is zero, the equation is as follows:

$$\frac{-V_{IO}}{R1} = \frac{V_{IO} - V_O}{R2}$$
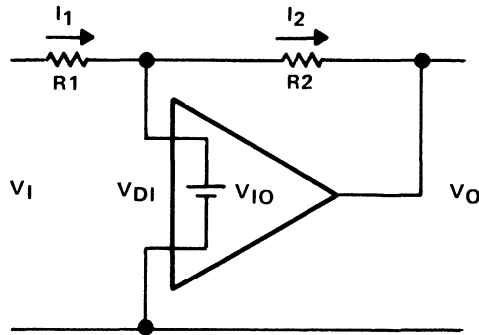
Fig. 2–6   Influence of Input Offset Voltage

The output voltage is the output offset voltage (V_{OO}). The following equation can be used to determine V_{OO}:

$$V_{OO} = \left(\frac{R2}{R1} + 1 \right) V_{IO}$$

The value of the input offset voltage can be found by dividing the output offset voltage by the closed-loop gain.

Input Offset Compensation

An ideal operational amplifier has zero input offset voltage and no drift. However, because of the mismatch of input transistors and resistors on the monolithic circuit, typical operational amplifiers have a low but definite offset voltage. Most single operational amplifiers have provisions for connecting an external potentiometer so that the input offset can be adjusted to zero. The exact method used and total resistance of the null adjustment potentiometer is dependent upon the type of operational amplifier circuit. A general-purpose internally compensated operational amplifier (a uA741) requires a 10 kΩ potentiometer. A BIFET or externally compensated operational amplifier requires a 100 kΩ potentiometer. Recommended input offset voltage null adjustment circuits are usually shown in the data sheet.

Examples of nulling the input offset voltage of the BIFET op-amps are shown in Figures 2–7 and 2–8. When the offset null pins (N1 and N2) are connected to the emitter of the constant-current generators,

used as the op-amp's first stage load, a circuit similar to that shown in Figure 2–7 is used. When the null pins are connected to the collectors of the constant-current generator, a circuit similar to that shown in Figure 2–8 is used.
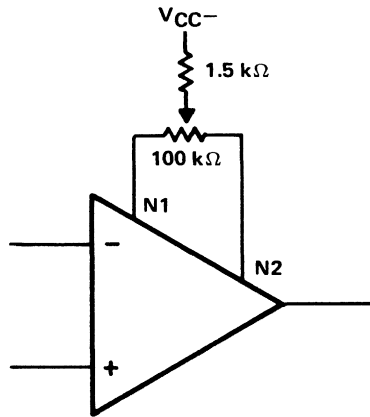
Fig. 2–7   Null Pins Connected to Emitters.
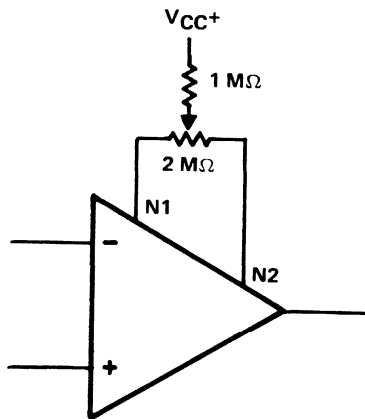
Fig. 2–8   Null Pins Connected to Collectors.

Actual resistor values and nulling circuits depend upon the type of operational amplifier used. Consult the appropriate data sheet for complete input offset nulling procedures.

Input Offset Voltage Temperature Coefficient

Input offset voltage temperature coefficient (offset voltage drift) is specified in volts per degree Celsius. The amount of drift that occurs with temperature variations is directly related to how closely matched the input characteristics are when the device is manufactured. BIFET input devices (such as the TL080 family) typically have 10 to 12 μV/°C. The LinCMOS^{TM} operational amplifier family has from 0.7 to 5 μV/°C depending upon the bias mode selected.

Influence of Input Bias Current

With no signal into the amplifier shown in Figure 2–9, input bias current flows through resistors R1 and R2. Because of the voltage drop across R1 and R2, these input currents will produce an offset voltage. Since the noninverting input is grounded, the voltage appears as input offset and is amplified by the operational amplifier.
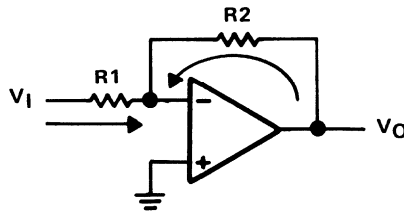
Fig. 2–9   Inverting Amplifier with Input Bias Currents.

The method commonly used to correct for a dc offset condition is to place an additional resistor (R3) between the noninverting input and ground.

The value of resistor R3 is calculated as the parallel combination of R1 and R2 as follows:

$$R3 = \frac{R1R2}{R1 + R2}$$

A voltage is developed across R3 that is equal to the voltage across the parallel combination of R1 and R2. Ideally, the voltages appear as common-mode voltages and are cancelled. However, in a typical

operational amplifier, the bias currents are not exactly equal. Because of this difference, a small dc offset voltage remains.

Influence of Input Bias and Offset Current Drift

Input bias current, and differential offset currents may drift with temperature. Although it is relatively easy to compensate for the effects of input bias current, correcting for drift with temperature variances is difficult. When drift tendencies are expected to be a design problem, device type, construction, and application should be considered.

Influence of Output Resistance

The influence of output resistance is illustrated by Figure 2–10.
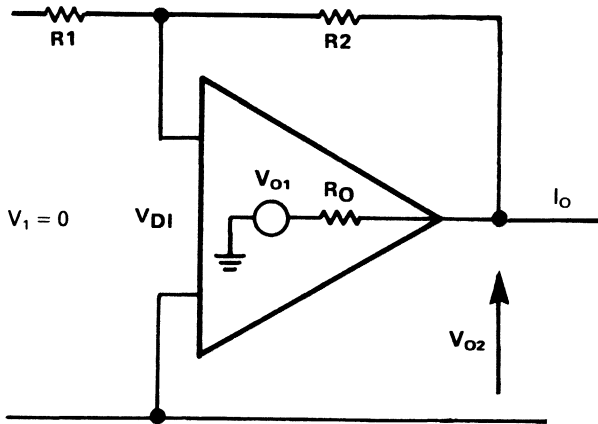
Fig. 2–10   Influence of Output Resistance.

If V_{O1} is the output voltage of the equivalent ideal amplifier, V_{O2} is the output voltage of the actual device and R_O is the op-amps output resistance then the output resistance R_{out} with feedback (shunt) can be expressed by the following:

$$V_{O1} = -A_{VD} \frac{R1\ V_{O2}}{R1 + R2} \text{ is the 'internal' output voltage}$$

adding the output voltage due to R_O

$$V_{O2} = -A_{VD}\frac{R1\,V_{O2}}{R1 + R2} + \left[I_O - \frac{V_{O2}}{R1 + R2}\right]R_O$$

collecting terms

$$I_O R_O = V_{O2}\left[1 + \frac{A_{VD}\,R1}{R1 + R2} + \frac{R_O}{R1 + R2}\right]$$

$$R_{out} = \frac{V_{O2}}{I_O} = \frac{R_O}{\left[1 + \dfrac{A_{VD}\,R1}{R1 + R2} + \dfrac{R_O}{R1 + R2}\right]}$$

As

$$\frac{R_O}{R1 + R2} \ll 1 + \frac{A_{VD}\,R1}{R1 + R2}\quad (A_{VD} \gg R_O)$$

$$R_{out} = \frac{R_O}{1 + \dfrac{A_{VD}\,R1}{R1 + R2}}\qquad \text{feedback factor } \beta = \frac{R1}{R1 + R2}$$

$$R_{out} = \frac{R_O}{1 + A_{VD}\,\beta}$$

Input Common-Mode Range

The input common-mode range may be defined as the maximum range of the input voltage that can be simultaneously applied to both inputs without causing cutoff, clipping, or saturation of the amplifier gain stages. The input stage must be capable of operating within its specifications over the dynamic range of output swing. If it cannot, the amplifier may saturate (or latch-up) when the input limits are exceeded. Latch-up occurs most often in voltage-follower stages where the output voltage swing is equal to the input voltage swing and the operational amplifier is driven into saturation. The specified common-mode voltage range of the input stage must exceed the maximum peak-to-peak voltage swing at the input terminals or the input stage may saturate on peaks. When saturation occurs, an inverting stage no longer inverts. The negative feedback becomes positive feedback and the stage remains in saturation.

Common-Mode Rejection Ratio (CMRR)

The common-mode rejection ratio may be defined as the ratio of the differential signal gain to the common-mode signal gain and is expressed in decibels.

$$CMRR = \frac{(\text{differential signal gain})}{(\text{common-mode signal gain})}$$

$$CMRR \text{ (dB)} = 20 \log_{10} \frac{V_O/V_{DI}}{V_O/V_{IC}} = \frac{V_{IC}}{V_{DI}}$$

This is measured by determining the ratio of a change in input common mode voltage ΔV_{IC} to the resulting change in input offset voltage ΔV_{IO} (ΔV_{DI}).

An ideal operational amplifier responds only to differential input signals and ignores signals common to both inputs. In a typical circuit, however, operational amplifiers have a small but definite common-mode error. Common-mode rejection is important to noninverting or differential amplifiers because these configurations see a common-mode voltage. Depending upon the type of device, dc rejection ratios may range from 70 dB to 120 dB.

Slew Rate

The slew rate may be defined as the maximum rate of change of the output voltage for a step voltage applied to the input (see Figure 2–11). Slew rate is normally measured with the amplifier in a unity gain configuration. Both slew rate and gain bandwidth product are measures of the speed of the operational amplifier.

$$SR \text{ (IN V/}\mu\text{s)} = \frac{\Delta E}{\Delta t}$$
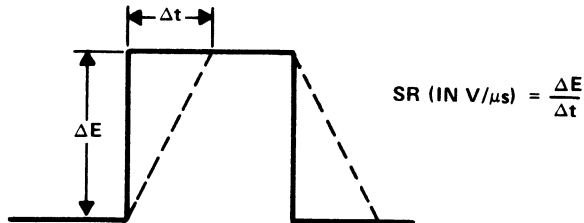
NOTE: Solid line is a square-wave input. Broken line is slewed input.

Fig. 2–11   Effect of Slew Rate.

Slew-rate limiting is the result of the op-amp's internal circuit's ability to drive the internal frequency compensation capacitor. The slew-rate performance of an op-amp limits the amplitude of the output voltage swing at higher operating frequencies.

When the current available to charge and discharge the internal capacitance becomes exhausted, slew-rate limiting occurs.

Noise

Operational amplifiers degrade the input signal by adding noise components. Noise components are usually random and determine the ultimate lower limit of signal-handling capability. Noise is usually specified on the data sheet as equivalent input noise, and like the other input factors, is increased by the gain of the stage. There are several potential sources of noise in an operational amplifier. The most common are thermal noise caused by the two source resistances (this noise exists within an ideal operational amplifier), internal noise current, and noise-voltage generators. Under normal audio applications the noise-voltage will be the dominant source of amplifier noise. As the source resistance is increased, the effect of noise-current increases until (at high source resistance) noise current and the bias compensation resistor noise together are the dominant components of amplifier input noise. In specifications, these two parameters are detailed separately. Noise voltage is specified at a low source resistance. Noise current is specified at a high source resistance. Both V_n and I_n are given in terms of spectral density. These are measured with a narrow-bandwidth filter (1 Hz wide) at a series of points across a useful spectrum of the amplifier. Data is usually given in terms of noise voltage versus frequency. Practical data or curves on data sheets are normally given as the following:

$$V_n = e_n/\sqrt{Hz}$$

NOTE: Typically a frequency and source resistance will be given in the test conditions included in the device data sheet.

In general, low-input-current operational amplifiers (BIFET, LinCMOS) or low-bias-current bipolar operational amplifiers will have lower noise current and tend to be quieter at source impedances above 10 kΩ. Below 10 kΩ, the advantage swings to bipolar operational amplifiers which have lower input voltage noise.

Phase Margin

Phase margin is equal to 180° minus the phase shift at the frequency where the magnitude of the open-loop voltage gain is equal to unity. Phase margin is measured in degrees and must be positive for unconditional stability. Figure 2–12 illustrates a typical circuit used to measure phase margin, and applies where loop gain is ≪1, that is $A_{OL} = A_{CL}$.
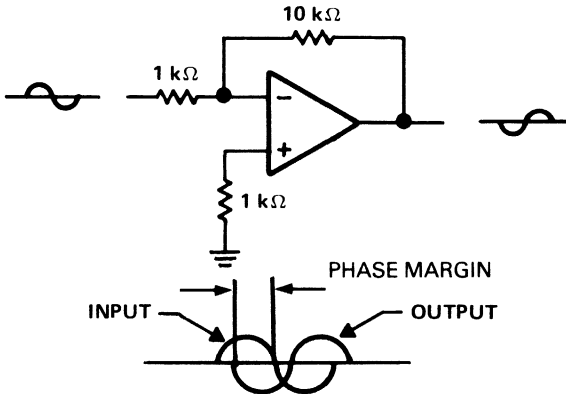
Fig. 2–12   Phase Margin Measurement Circuit.

If the phase difference between the input and output waveform is 120° (after the 180° due to negative feedback has been subtracted), 180° minus 120° phase difference leaves 60° as the phase margin. Phase margin will normally be from 50° to 70° on commercially available operational amplifiers. When the phase margin decreases to 45°, the operational amplifier approaches instability. This is indicated by both a peak in the amplitude response at the band edge and ringing in the transient response.

Output Voltage Swing (V_{OPP})

V_{OPP} is the peak-to-peak output voltage swing that can be obtained without clipping or saturation. Peak-to-peak swing may be limited by loading effects, operational amplifier slew rate capability, load resistance, and power supply used. Load resistances given on the data sheet

are usually 2 kΩ or 10 kΩ. With load resistances of 2 kΩ or less, the output decreases due to current limiting. Normally, this will not damage the operational amplifier as long as the specified power-dissipation limits of the package are not exceeded. However, the open-loop gain will be reduced because of excessive loading.

Feed-Forward Compensation

Operational amplifiers have high gain input stages and often use lateral PNP transistors (which have poor high frequency performance) in this part of the circuit. If this stage can be bypassed for high frequencies only the subsequent lower gain, wider bandwidth stages can amplify high frequencies and extend the overall frequency response.

A 500pF feed-forward capacitor connected from the inverting input (pin 2) to the compensation input (pin 1), as shown in Figure 2–13, feeds the high frequency signal around the input stage in contrast to the more usual feedback.
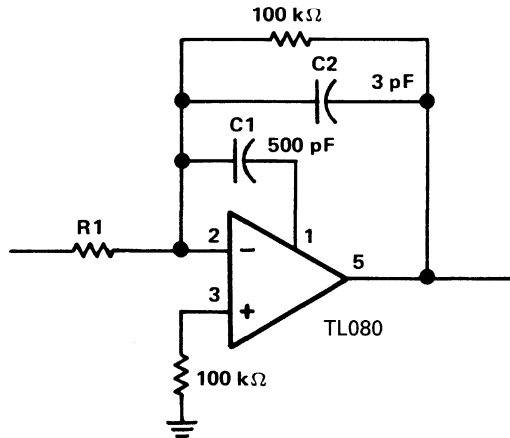
Fig. 2–13   Feed-Forward Compensation.

The example shown uses a TL080 BIFET and the response curves of Figure 2–14 show an increase in bandwidth at a closed loop gain of 60 dB from 6 kHz to 200 kHz.

**OPEN-LOOP LARGE SIGNAL
DIFFERENTIAL VOLTAGE GAIN
vs
FREQUENCY**
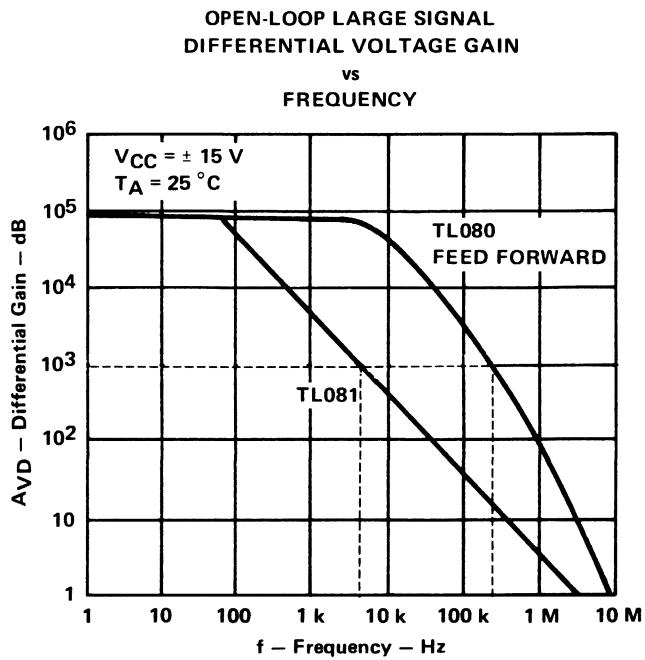
Fig. 2–14   Feed-Forward Compensation Curves.

The TL080 provides for externally controlled compensation on pins 1 and 8. This is an advantage over the internally compensated version (TL081) because it allows the user to obtain slew rates from a typical 12 V/μs (for nominal compensation of 12 pF) to 30 V/μs (for a compensation of 3 pF). This increased slew rate is also reflected in the small signal response where the rise time is decreased from 0.1 μs to less than 50 ns. The power bandwidth can be extended to greater than 1 MHz. This greatly increases the potential for large-signal wide-bandwidth applications and for filters with frequencies at or above 1 MHz. The unity gain bandwidth is identical to the normal compensation mode but the first pole frequency is extended above 10 kHz; thus, gain accuracy is maintained at higher frequencies.

BASIC OPERATIONAL AMPLIFIER CIRCUITS

Operational amplifiers, have a wide range of adaptability and can be configured to perform a large number of functions. Operational

amplifier applications are frequently limited more by the imagination than by their functional limitations or operating parameters. The basic operational amplifier circuits that are discussed in this section are as follows:

- ● Noninverting Amplifier

- ● Inverting Amplifier

- ● Summing Amplifier

- ● Differentiator

- ● Active Filter

- ● Voltage Follower

- ● Differential Amplifier

- ● Integrator

Noninverting Operational Amplifier

A noninverting amplifier circuit provides an amplified output that is in phase with the circuit input. Figure 2–15 illustrates a basic noninverting operational amplifier circuit. In the circuit shown in the figure, the output is in phase with the input at low frequencies, becoming $-45°$ at the -3 dB bandwidth.
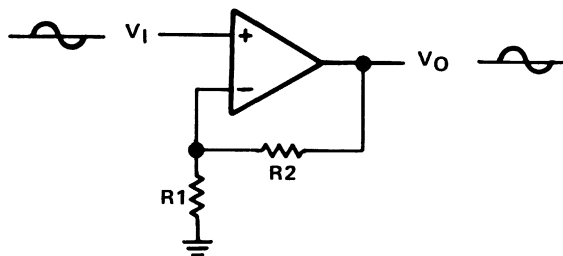
Fig. 2–15   Basic Noninverting Amplifier Circuit.

In this circuit, the input signal is applied to the noninverting ($+$) input of the amplifier. A resistor (R1), which is usually equal to the resistance of the input element, is connected between ground and the

inverting (−) input of the amplifier. A feedback loop is connected from the output of the amplifier, through feedback resistor R2, to the inverting input. The voltage gain of a noninverting amplifier circuit is always greater than unity.

The input impedance of this circuit, with feedback applied in series with the input voltage, is R1 $(1 + \beta A_{OL})$ where

$$\beta = \frac{R1}{R1 + R2}$$

The output of the noninverting amplifier circuit can be determined by the following equation:

$$V_O = \left[1 + \frac{R2}{R1} \right] (V_I)$$

The voltage gain of the noninverting amplifier circuit can be determined by the following equation:

$$A_V = \frac{V_O}{V_I} = 1 + \frac{R2}{R1}$$

Inverting Amplifiers

An inverting amplifier circuit, as illustrated in Figure 2–16, provides an output that is 180 degrees out of phase with the input signal.
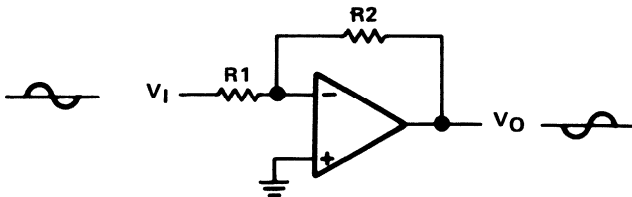
Fig. 2–16   Basic Inverting Amplifier Circuit.

In this circuit, the input signal is applied through a resistor (R1) to the inverting input (−) of the operational amplifier. The noninverting

input (+) is connected to ground. Feedback is connected from the output, through feedback resistor R2, to the inverting input. The voltage gain of an inverting amplifier circuit can be less than, equal to, or greater than unity.

Resistor R1 provides the input impedance of the inverting amplifier circuit due to the 'virtual' earth existing at the inverting input. The input impedance is much lower than for a noninverting amplifier circuit.

The output voltage for an inverting amplifier can be determined by the following equation:

$$V_O = \left[-\frac{R2}{R1} \right](V_I)$$

NOTE: The minus sign in the equation indicates the 180° phase reversal.

The voltage, or closed-loop, gain can be determined by the following equation:

$$A_{CL} = \frac{V_O}{V_I} = -\left[\frac{R2}{R1} \right]$$

Voltage Follower

The voltage or source follower is a unity-gain, noninverting amplifier with no resistor in the feedback loop (see Figure 2–17). The output is exactly the same as the input. The voltage follower has a high input impedance which is equal to the operational amplifier's intrinsic input impedance, R1, multiplied by $(1 + A_{OL})$.
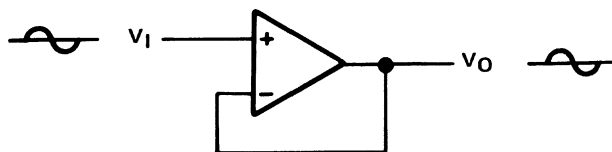
Fig. 2–17   Basic Voltage Follower Circuit.

The function of the op-amp voltage follower circuit is identical to an emitter follower for a bipolar transistor or a source follower on a FET transistor, but gives a gain much closer to unity because of the op-amp's inherent higher gain. The main purpose of the circuit is to buffer the input signal from the load. The input impedance is high and the output impedance is low.

Summing Amplifier

If several input resistors are connected to the inverting input of the operational amplifier, as shown in Figure 2–18, the result is an amplifier which sums the separate input voltages.
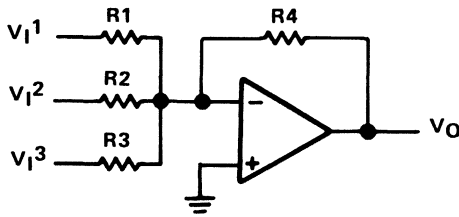
Fig. 2–18   Basic Summing Amplifier.

The output voltage of the summing amplifier circuit can be determined by the following equation:

$$V_O = -R4 \left(\frac{V_I1}{R1} + \frac{V_I2}{R2} + \frac{V_I3}{R3} \right)$$

If feedback resistor R4 and input resistors R1, R2 and R3 are made equal, the output voltage can be determined by the following equation:

$$V_O = - (V_I1 + V_I2 + V_I3)$$

Difference Amplifier

In a difference amplifier circuit, input voltages V_I1 and V_I2 are applied simultaneously to the inverting and noninverting inputs of the operational amplifier (see Figure 2–19).
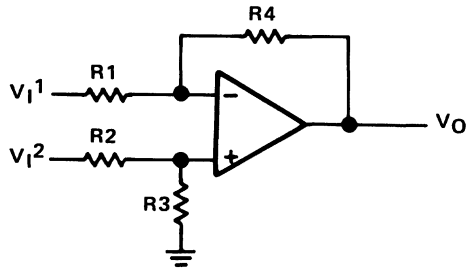
Fig. 2–19   Basic Difference Amplifier Circuit.

When all four resistors are equal, the output voltage is equal to the difference between V_I2 and V_I1. This circuit is called a unity-gain analog subtractor. Mathematically, the output voltage is stated as follows:

$$V_O = V_I2 - V_I1$$

Differentiator

The operational amplifier differentiator is similar to the basic inverting amplifier circuit except that the input component is a capacitor rather than a resistor (see Figure 2–20).
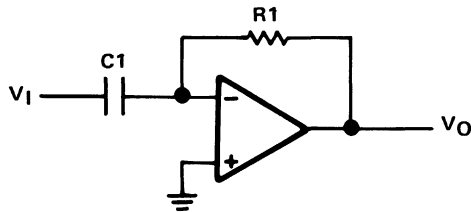
Fig. 2–20   Basic Differenciator Circuit.

The output voltage of the differentiator circuit can be determined by the following equation:

$$V_O = -R1C1\frac{\Delta V_I}{\Delta t}$$

In this equation $\Delta V_I/\Delta t$ is the change in input voltage divided by a specified time interval. A problem with the basic differentiator circuit is that the output voltage increases with frequency and makes the circuit susceptible to high-frequency noise. To compensate for this problem, a resistor is connected in series with the capacitor on the inverting input limiting the high frequency gain (see Figure 2–21).
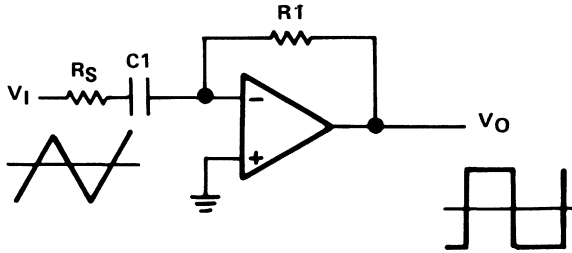
Fig. 2–21   Differentiator with High Frequency Noise Correction.

This circuit functions as a differentiator only on input frequencies which are less than those which can be determined by the following equation:

$$fC1 = \frac{1}{2\pi R_S C1}$$

The time constant ($R_S C1$) should be approximately equal to the period of the input signal to be differentiated. In practice, series resistor R_S is approximately 50 Ω to 100 Ω.

Integrator

An operational amplifier integrator circuit can be constructed by reversing the feedback resistor and input capacitor in a differentiator circuit (see Figure 2–22).
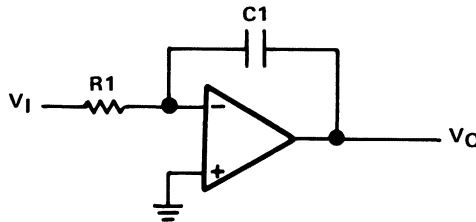
Fig. 2–22   Basic Integrator Circuit.

The resistor (R1) is the input component and the capacitor (C1) is the feedback component. However, if the low-frequency gain of the circuit is not limited, the dc offset (although small), would be integrated and eventually saturate the operational amplifier. A more practical integrator circuit is shown in Figure 2–23.
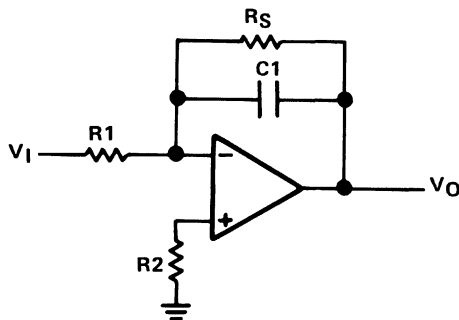
Fig. 2–23   Typical Integrator Circuit.

In this circuit, a shunt resistor (R_S) is connected across feedback capacitor C1 to limit the low-frequency gain of the circuit. The dc offset (due to the input bias current) is minimized by connecting resistor R2 between the noninverting input and ground. Resistor R2 is equal to the parallel combination of R1 and shunt resistor R_S. The shunt resistor helps limit the circuit low-frequency gain for input frequencies greater than those determined by the following equation.

$$fC1 = \frac{1}{2\pi\,R_S C1}$$

CHOOSING THE RIGHT OPERATIONAL AMPLIFIER

The operational amplifier, because of its versatility and ease of application, is the most widely used linear integrated circuit today. This useful linear building block has made many electronic circuits much less complex. Due to the popularity of the operational amplifier, many different types are available that offer a variety of features. Which device to use for a specific application is a question that must be answered. If the characteristics of the selected device are not adequate, total system performance may be less than desired. If the selected device is too complex for the job, system cost may be increased

unnecessarily. The following paragraphs provide a summary of the various types of operational amplifiers. To assist in the selection of the most effective operational amplifier for a specific application, the features and key applications are presented.

General Purpose Operational Amplifiers – Bipolar

The key features of a bipolar operational amplifier are as follows:

Input impedance of 10^6 Ω.

Typical slew rates from 0.5 to 1 V/μs.

Typical unity-gain bandwidth of 1 MHz.

Noise levels of approximately 25 to 30 nV/$\sqrt{Hz}$.

Table 2–1 is a selection guide showing the major parameters to be considered in choosing bipolar operational amplifiers for a particular circuit design.

Table 2–1   Bipolar Operational Amplifier Comparison Chart.

PARAMETER	DEVICE									UNITS
	OP-07	741	TL321	SE5534A	LM358	LM318	MC1458	RC4136	RC4558	
V$_{IO}$	30 µV	1	2	0.5	2	2	1	0.5	0.5	mV
I$_{IO}$	0.5	20	5	10	5	30	20	5	5	nA
I$_B$	± 1.2	80	45	400	45	150	80	40	40	nA
SR	0.2	0.5	0.5	6	0.5	70	0.5	1	1	V/µs
B1	0.6	1	1	10	1	15	1	3	3	MHz

[†]Test conditions are V$_{CC}$ = ± 15 V. All values are typical.
[‡]Unity-gain bandwidth

BIFET Operational Amplifiers

BIFET operational amplifiers combine JFET input transistors with bipolar transistors in a monolithic integrated circuit. The ion-implantation process used in making BIFET devices results in closely matched input transistors and permits the manufacture of cost effective op-amps with a performance superior to all bipolar designs.

In addition to high input impedance ($10^{12}\Omega$) and input bias currents in the picoampere range, the TL070/TL080 series BIFET operational amplifiers have slew rates of approximately 13 V/μs and a typical unity gain bandwidth of 3 MHz.

Another feature of the TL070/TL080 series BIFET is the true class-AB operation in the output stage which results in near zero crossover distortion and low total harmonic distortion.

Some BIFET operational amplifiers are power-adjustable. This allows the user to select (with an external resistor) the operating current levels. This allows a tradeoff between power dissipation, and slew rate or signal bandwidth. An example of such a device is the TL066 BIFET operational amplifier. The TL066 can be adjusted for a no-signal supply current of 5 to 200 μA. Slew rate and bandwidth will also change depending upon the level of operating current. Except for the adjustable feature, the TL066 is similar to the TL061. The key application for power adjustable operational amplifiers is in battery-operated and telecommunication equipment where power consumption is an important factor. Table 2–2 is a selection guide listing the major parameters to be considered when choosing a BIFET operational amplifier for a particular application.

Table 2–2   BIFET Operational Amplifier Comparison Chart.

PARAMETER	DEVICE SERIES				UNITS
	TL080	TL070	TL060	TL087	
V_{IO}	5	3	3	0.1	mV
I_B	30	30	30	60	pA
NOISE	25	18	42	18	nV/Hz
SR	13	13	3.5	13	V/μs
B1	3	3	1	3	MHz

Test conditions are $V_{CC} = \pm15$ V. All values are typical.

LinCMOS^{TM} Operational Amplifiers

The linear silicon-gate CMOS integrated circuit process and technology combines the high speed of the bipolar device with the low power, low voltage, and high input impedance of the CMOS device. In addition, the LinCMOS device overcomes the stability limitations imposed on linear designs by metal-gate CMOS.

Ultrastable Offsets

The primary disadvantage of using conventional metal-gate CMOS for linear applications is the unavoidable threshold-voltage shifts that take place with time and with changes in temperature and gate voltage. These shifts (caused by the movement of sodium ions within the gate oxide) are frequently more than 10 mV/V of applied gate voltage. However, LinCMOS technology overcomes this problem by replacing the metal gates with phosphorus-doped polysilicon gates that bind the sodium ions. The result is linear integrated circuits with low (2 to 10 mV) input-offset voltages that vary no more than a few microvolts from their original values.

The TLC251 and TLC271 series of general-purpose operational amplifiers have low input offset voltages that typically vary only 0.1 μV per month and 0.7 μV per degree Celsius. The offset voltage can be reduced by using the offset null pins on the device. Unlike metal-gate CMOS devices, the input-offset voltage of LinCMOS devices is not sensitive to input-overdrive voltages.

Wide Bandwidths

In addition to providing stable offset voltages, LinCMOS technology produces integrated circuits with bandwidths that are two to three times wider than those of metal-gate CMOS devices. This occurs because in the LinCMOS process the Silicon gate of the p and n MOS transistors is formed during the same processing step that forms the source and drain. As a result, the source, gate, and drain are self-aligned. In contrast, metal gates are formed after the source and drain regions are diffused, necessitating a built-in overlap to ensure source, gate, and drain alignment.

The self-aligned gate of LinCMOS transistors results in a gate-drain capacitance that is approximately one-seventh that of typical metal-gate CMOS integrated circuits. This enhances the bandwidth and speed of LinCMOS devices.

The TLC251 and TLC271 operational amplifiers offer a 2.3 MHz bandwidth, 60-ns rise-time with 25% overshoot, and a slew rate of 4.5 V/μs. These speeds are better than most bipolar operational amplifiers, approach those of BIFET operational amplifiers, and are several times faster than their metal-gate CMOS counterparts.

Advantages of LinCMOS Operational Amplifiers

The TLC251 and TLC271 series operational amplifiers allow selection of low-, medium- or high-bias operation. This is accomplished by connecting the bias-select pin to V_{DD} for low bias, to ground for high bias, or to a voltage 0.8 Volts inside either supply rail for medium bias. By providing a choice of bias conditions, the TLC251 and TLC271 allow users to select between ac performance and power consumption to meet a wide range of circuit requirements. When operated in high-bias with V_{DD} equal to 10 V, these devices draw 1000 μA of I_{DD} for 10 mW power dissipation and feature 4.5 V/μs slew rate and 2.3 MHz bandwidth. In the low bias mode with V_{DD} equal to 10 V and I_{DD} equal to 10 μA (100 μW power dissipation), the devices have a slew rate of 0.04 V/μs and a bandwidth of 100 kHz. In low-bias, and at 1 V, the TLC251 consumes just 10 μW making it the ideal choice for battery-operated applications. The bias-select pin can be driven with a logic signal from a microprocessor, allowing the operational amplifier performance to be software-controlled.

Additional features of the TLC251 and TLC271 include a common-mode rejection ratio of 88 dB and a low input-noise voltage of 30 to 70 nV/$\sqrt{Hz}$ (depending upon whether the device is operating in high, medium, or low bias).

These capabilities make the TLC251 and TLC271 suited for a wide range of applications. These applications include active filters, transducer interfacing, current drivers, voltage-to-current converters, long-interval timers, and many types of amplifiers. The TLC251 and TLC271 series are particularly suited for low supply voltage and low-power designs.

When using the TLC251 or TLC271 LinCMOS devices for design, the following characteristics must be considered:

- Supply Voltage, V_{DD}
  TLC251 .... 1 V to 16 V
  TLC271 .... 3 V to 16 V

- True Single Supply or a Maximum of ±8 V

- Selectable Supply Current, I_{DD}
  Low Bias = 10 μA typical
  Medium Bias = 150 μA typical
  High Bias = 1000 μA typical

● Extremely Low Input Bias and Offset Currents: 1 pA Typical

● Low Input Offset Voltage: 3 mV typical

● Ultra Stable Input-offset Voltage:
  0.1 μV/Month Typical

● Noise: 30 nV/Hz Typical (High bias)

● Slew Rate, SR
  High Bias . . . . 4.5 V/μs typical
  Medium Bias . . . . 0.6 V/μs typical
  Low Bias . . . . 0.04 V/μs typical

● Bandwidth, BW
  High Bias . . . . 2.3 MHz
  Medium Bias . . . . 0.7 MHz
  Low Bias . . . . 0.1 MHz

COMPARATORS

A basic comparator is a differential amplifier with typically either an open collector or TTL compatible output stage operating in the open-loop mode. Because of high gain, the output is normally saturated in either the high state or the low state depending upon the relative amplitudes of the two input voltages. With these conditions, the comparator provides a logic-state output which is indicative of the amplitude relationship between two analog input signals.

Figure 2–24 illustrates a basic comparator and its transfer function.
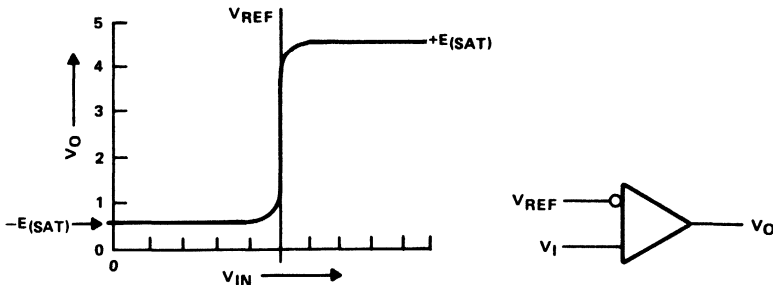
Fig. 2–24   Basic Comparator and Transfer Function.

In the circuit in Figure 2–34, if a reference voltage is applied to the inverting input and an unknown potential to the noninverting input, the output will reflect the relationship between the two inputs. When V_I is more negative than V_{REF}, the device output will be in saturation at a logic low level. When V_I becomes more positive than V_{REF}, the output will change states and become saturated at a logic high level or off for an open collector output.

Because comparators are normally used to drive logic circuits, the output must change states as rapidly as possible. High open-loop gain, wide bandwidth and slew rate are key factors in comparator speed.

Circuits designed as a comparator use none of the phase/frequency compensation usually required for operational amplifier stabilization with feedback. In fact, these compensation components are detrimental because they slow the response time of the comparator. Although any operational amplifier may be used as a comparator, a compensated device (such as the TL071) will result in longer response times.

The ideal comparator has characteristics that are similar to an ideal operational amplifier, except the comparator is not optimised for closed loop operation. These characteristics are as follows:

● Differential Gain = $\rightarrow \infty$

● Common-Mode Gain = 0

● Input Impedance = $\rightarrow \infty$

● Output Impedance = 0

● Bandwidth = $\rightarrow \infty$

● Offset Voltage and Current = 0

Comparator Parameters

Some of the common comparator parameters are discussed in the following paragraphs.

Source Impedance

The input bias current of a bipolar comparator is approximately in the range -0.25 to 20 μA. When the differential input voltage makes

the comparator switch, the input bias current is present at one of the inputs and is almost zero at the other. If the source impedances are not negligible, the bias current switching will cause changes in the comparator input levels and create parasitic oscillations.

Figure 2–25 shows this phenomenon occuring with a TL810. The comparator is driven by a ramp voltage at a rate of 1 mV/μs as represented by the centre waveform. The upper output waveform shows the response of the comparator with a source impedance of 50 Ω. The lower output waveform represents the response of the same comparator with a source impedance of 10 kΩ. The initial switching occurs sooner with a high source impedance because the bias current characteristics produce an additional offset voltage. However, the subsequent oscillations make this circuit configuration unusable with low-slew-rate input signals.
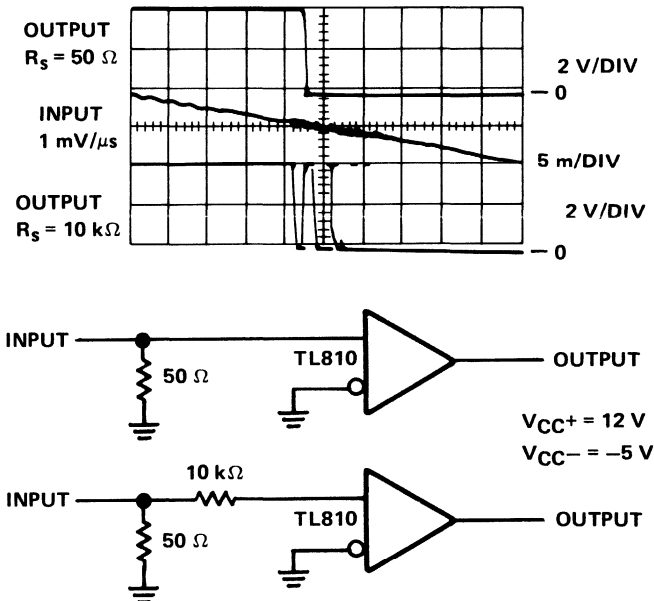
Fig. 2–25   Influence of Source Impedance.

TLC3__ series ·comparators manufactured using the LinCMOS process overcome these problems with their very low bias currents typically, 1 pA. Also their very high input impedance, in the order of 10^{12} ohms, make them very suitable for use with high source impedances.

Differential Voltage Gain

Differential voltage gain (A_{VD}) determines the sensitivity and threshold accuracy of a comparator. In the ideal comparator, the gain would be inifinite and an extremely small voltage applied between the two inputs would cause a change in the output. In actual practice, the gain is not infinite and some minimum voltage variation at the input is required to obtain a change in the output. The ratio of the variation of output voltage to that of input voltage is the voltage gain of the comparator. The voltage gain of the comparator may be expressed by the following equation:

$$A_{VD} = \frac{\Delta V_O}{\Delta V_I}$$

For example, a comparator with a TTL compatible output has the quantity ΔV_O (difference between the high and low states of the output) normally set at 2.5 V to ensure matching between the comparator and a TTL load. That is, if the TL810 has a minimum A_{VD} of 12 500, then (for an output swing of 2.5 V) ΔV_I (min) = 2.5 V/12 500 or 0.2 mV.

Output Characteristics

Output stages of comparators take one of three forms:

1) Push-pull to give either TTL or HCMOS compatible output levels.

2) Uncommitted pull-down, either open collector or open drain for bipolar and CMOS technology respectively.

3) Uncommitted transistor with both emitter and collector outputs available.

In the range of TLC3__ series LinCMOS comparators there are devices which have push-pull outputs or open drain.

There are bipolar comparators available which encompass all three types of output circuit.

For TTL some comparators have a full fanout capability of 10 or greater, others have a fanout that is limited to one TTL load. An evaluation of the output circuits should indicate the basic limiting factors and how maximum performance can be obtained.

For example, the TL810 in the active pull-down mode (see Figure 2–26(a)), has an output low-level sink current (I_{OL}) that is limited. The emitter of Q2 is clamped at one base-emitter voltage drop or -0.7 V with Q3 providing another base-emitter voltage drop.

(a) TL810 LOW STATE   (b) TL810 HIGH STATE

(c) TL811 FANOUT OF 2
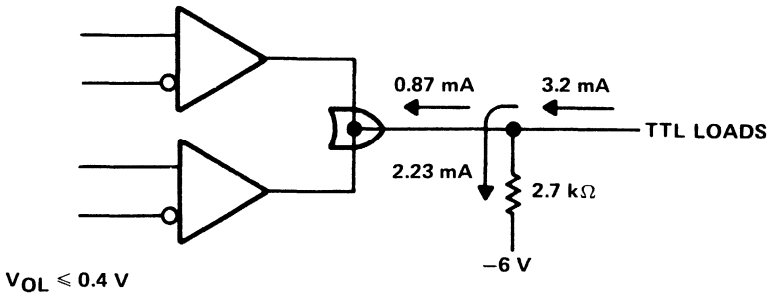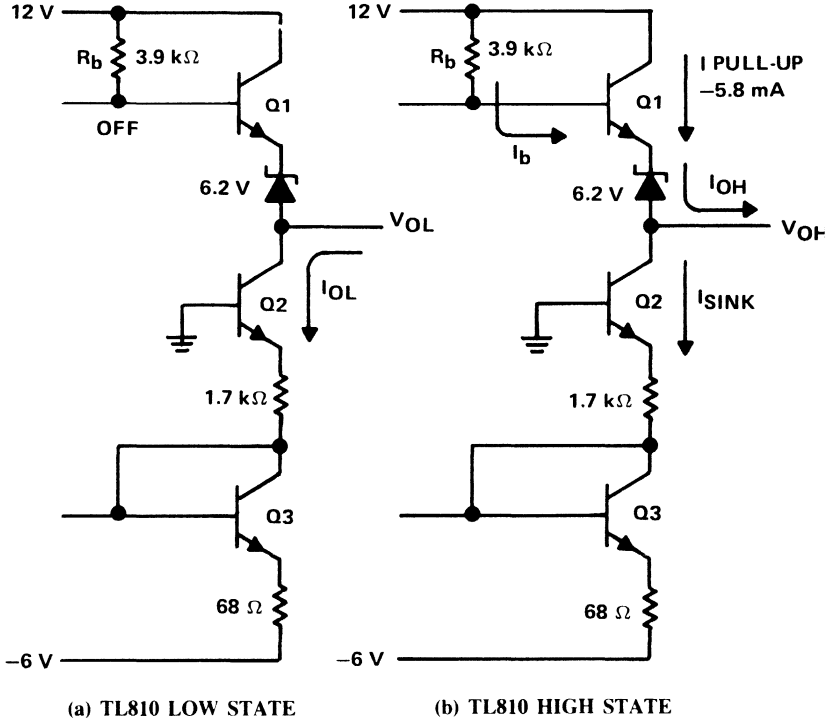
Fig. 2–26   Comparator Output Configurations.

The resulting low-level output current (I_{OL}) may be calculated from the following equation:

$$I_{OL} = \frac{V_{CC} - 2\,V_{BE}}{1.77\ k\Omega}$$

$$= \frac{-6\ V + 1.4\ V}{1.77\ k\Omega} = -2.6\ mA$$

The resulting value is near the typical value for this device. The minus sign indicates a sink current. The corresponding $V_{OL} = V_E$ (Q2) + $V_{CE(SAT)}$(Q2) or (-0.7 V + 0.2 V) = -0.5 V, which is the typical data sheet value.

In a logic low-level output state, the TL810 can handle one standard TTL gate with its maximum requirement of -1.6 mA. Increased fanout capability can be obtained by connecting an external resistor between the comparator output and the negative supply.

In the active pull-up mode, the typical high-level output voltage (V_{OH}) is 3.2 V for the TL810. The voltage at the base of the pull-up transistor [Q1, Figure 2–26(b)] is defined by the following equation:

$$V_{OH} + V_Z + V_{BE(Q1)}$$

Where:

$$V_Z = 6.2\ V$$

$$V_{BE(Q1)} = 0.7\ V$$

The base voltage is (3.2 + 6.2 + 0.7), 10.1 V. The resulting base drive is determined by the following equation:

$$I_b = \frac{V_{CC+} - V_B}{R_b}$$

$$= \frac{12\ V - 10.1\ V}{3.9\ k\Omega} = 0.488\ mA$$

Assuming a typical saturated h_{FE} of 12, the resulting pull-up drive capability is (0.488 mA) (12) or 5.8 mA. Only part of the 5.8 mA drive

is available to the external circuit. Since the current sink is not turned off during the logic-high output condition, the remainder of the current will be shunted through the pull-down circuit. For TL810, the resulting I_{OH} level available for external drive will be the difference between the pull-up drive of -5.8 mA and the pull-down sink of 2.6 and is -3.2 mA [Figure 2–26(c)]. The -3.2 mA is adequate because the logic high level (I_{OH}) required is only 40 μA per TTL load. Similar calculations for the TL811 comparator yield an I_{OL} level of 0.87 mA and an I_{OH} of -4.3 mA. For example, a fanout capability of 2 requires an I_{OL} level of 3.2 mA. With the TL811 [see Figure 2–26(c)], a 2.7 kΩ resistor is connected between the output and the negative supply. The resulting I_{OL} is 3.2 mA at a 0.4 V maximum V_{OL}. The effective I_{OH} capability, therefore, is reduced to -1.19 mA at a minimum V_{OH} of 2.4 V.

The LM311 is a popular bipolar device that will operate from single or dual supplies from 5 V to 30 V (or ±15 V). The LM311 has an uncommitted output transistor with an available emitter and collector. This allows source or sink output drive. The output is compatible with most standard logic levels.

Figure 2–27 is a basic diagram of the LM311 comparator.

PIN NUMBERS SHOWN ARE FOR
8-PIN DUAL-IN-LINE PACKAGE.
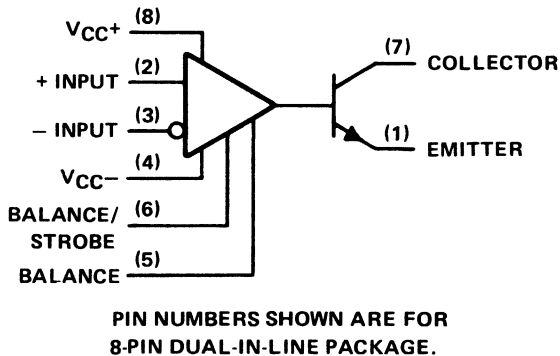
Fig. 2–27   LM311 Comparator.

Use of Hysteresis

Applications in which the input signal to the comparator slowly varies can cause the output to chatter. This becomes a problem when

the comparator is used to trigger a logic stage requiring fast rise and fall inputs. One solution to the problem is the introduction of positive feedback. This causes a fast or Schmitt trigger action. This action is accomplished by feeding a portion of the output signal back to the noninverting input. With the introduction of positive feedback, a different trip-level will be introduced for each transition. The result is two (rather than one) threshold points. These are called the upper threshold point (UTP) and lower threshold point (LTP), the difference between these two points is the hysteresis. A comparator with hysteresis is shown in Figure 2–28.
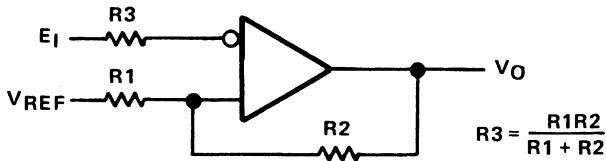
Fig. 2–28   Comparator with Hysteresis.

A typical hysteresis loop diagram for this type of circuit is shown in Figure 2–29.
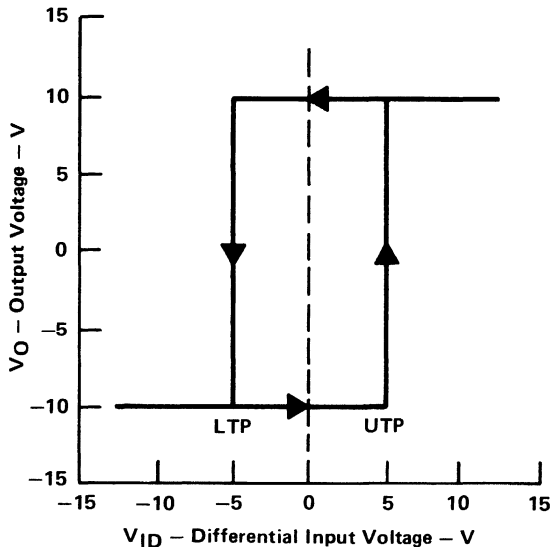
Fig. 2–29   Typical Comparator Hysteresis Loop.

Application Precaution

As previously discussed the rise time of the input signal is a critical parameter in some comparator applications. When using comparators with TTL outputs it is necessary to make sure that the output transition is fast enough as this type of logic requires switching times of less than 150 ns to function correctly without going into oscillation. The comparator input signal must have a minimum rate of change to avoid this problem.

Figure 2–30(a) shows the output of a TL710 being driven by a ramp voltage which varies at approximately 0.1 mV/μs. The switching times of the output, taken between 0.8 V and 2 V, are approximately 10 μs for the fall and rise times. In this mode, the output of the comparator is not compatible with TTL circuits.

OUTPUT
—0 2 V/DIV

INPUT
—0 5 mV/DIV

20 μs/DIV

(a) TL710

OUTPUT
—0 2 V/DIV

INPUT
—0 5 mV/DIV

20 μs/DIV
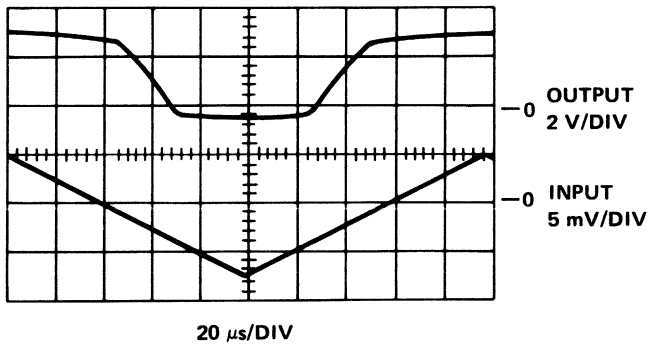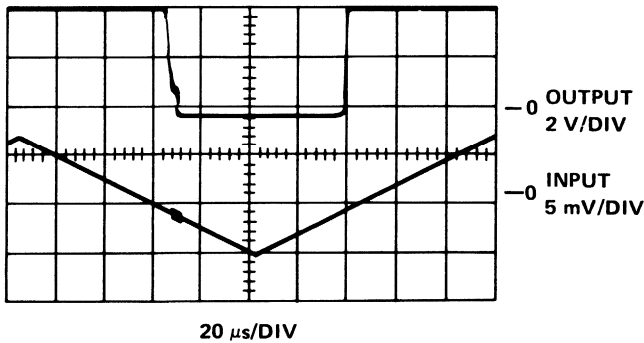
(b) TL810

Fig. 2–30   Response of a TL710 and a TL810 to a Ramp Input.

Figure 2–30(b) shows a TL810 under the same conditions as described for the TL710. With a higher gain than the TL710, the switching speed for the TL810 is also higher, and the rise time is compatible with TTL circuits. However, some oscillation is present during the periods of switching. This occurs because the input signal remains in the high-gain linear range of the comparator for an excessive period of time. For the output of a comparator to be good, the input must force the output to vary between 0.8 V and 2 V in 150 ns or less.

When the minimum gain (A_{VD}) of the comparator is known, the input signal must vary at a minimum rate determined by the following equation:

$$\frac{2\,V - 0.8\,V}{150\,ns \times A_{VD}}$$

For the TL710, the minimum rate is determined as follows:

$$\frac{2\,V - 0.8\,V}{150\,ns \times 500} = 16\,mV/\mu s$$

For the TL810, the minimum rate is determined as follows:

$$\frac{2\,V - 0.8\,V}{150\,ns \times 8000} = 1.0\,mV/\mu s$$

When these input conditions are not being met, some positive feedback must be added or a Schmitt trigger configuration must be designed (see Figure 2–31) to accelerate the switching speed. However, the resulting hysteresis makes the comparator less voltage sensitive.
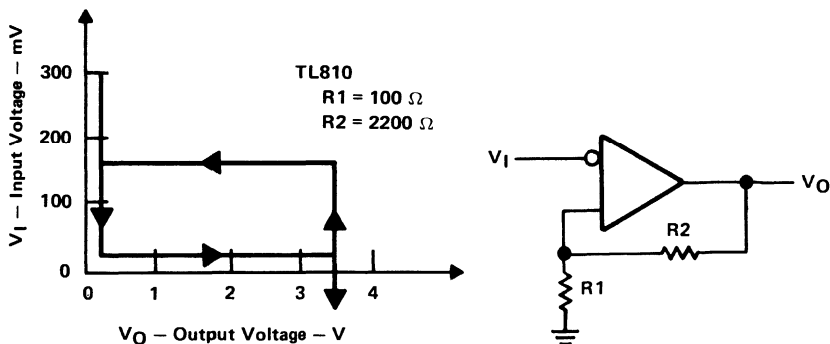
Fig. 2–31   Use of Hysteresis to Prevent Oscillations.

Section 3

Operational Amplifier and Comparator Applications

OPERATIONAL AMPLIFIER APPLICATIONS

General Applications

This section is intended to assist the reader in designing circuits incorporating operational amplifiers. The function that these circuit examples perform include: amplification, measurement, control, sensing and regulation and can be applied to a variety of applications. The section also contains sufficient information to allow the design of circuits for additional applications.

The following circuits are discussed in this section:

● Optical Sensor to TTL Interface

● Bridge-Balance Indicator

● High-Input-Impedance Differential Amplifier

● Low-Voltage Shunt Limiter

● PTC Thermistor Automotive Temperature Indicator

● Accurate 10-Volt Reference

● Precision Large Signal Voltage Buffer

Optical Sensor to TTL Interface Circuit

This optical sensor to TTL interface circuit is designed to detect a low light level at the sensor, amplify the signal, and provide a TTL-level output. When the optical sensor detects low-level light (ON condition), its output is small and must be amplified. Because of this small output, an operational amplifier with very low input bias current and high input resistance must be used to detect the ON condition of the sensor and provide an amplified output.

Figure 3–1 is an optical sensor to TTL interface circuit. When connected as shown in the figure, operational amplifier TL081 BIFET meets all of the previously stated characteristics. When sensor TIL406 is in the ON condition, its output is assumed to be 250 nA (allowing a safety margin). This results in a 250 mV signal being applied to the noninverting input of amplifier TL081. Because of the circuit configuration, the TL081 provides a gain of 100 and its output is in positive saturation. The TL081 output level is applied to a loading network that provides the basic TTL level. Because a TL081 optoelectronic circuit may operate at slow speeds, it may be necessary to connect an SN7413 Schmitt-trigger device on the output of the load network to shape the TTL output signal.

CONDITION	TIL406 CURRENT	OUTPUT LOGIC
LIGHT ON	≈ 3 μA	0
LIGHT OFF	≈ 3 nA	1
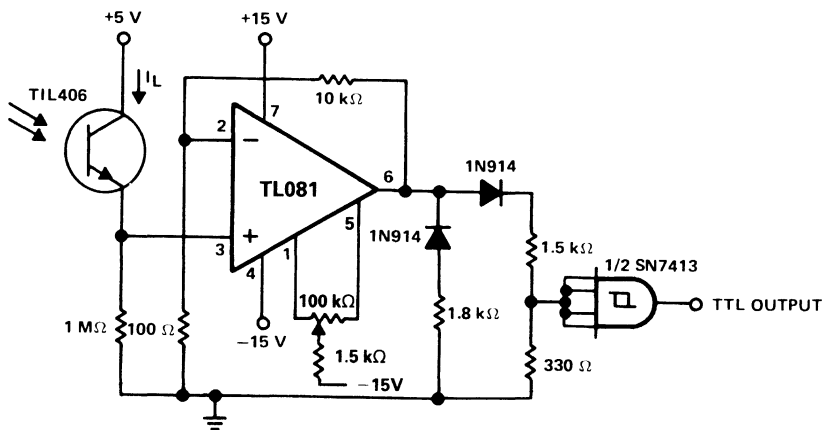
Fig. 3–1   Optical Sensor to TTL Interface Circuit.

Bridge-Balance Indicator

A bridge-balance indicator provides an accurate comparison of two voltages by indicating their degree of balance (or imbalance).

A common bridge, referred to as a Wheatstone bridge, consists of two impedance divider networks as shown in Figure 3–2. Generally one side of the bridge consists of known impedances (one of which is usually adjustable) resulting in a known voltage (E1). The other side of the bridge may consist of combined known and unknown impedances resulting in an unknown voltage E2. The unknown impedance might be varied by a system condition (speed, temperature, etc.). A sensitive voltmeter is used to detect the balance of E1 and E2. For example, the bridge may be used to control motor speed, temperature, or physical position. The accuracy of this type of control is dependent on how close to zero difference, or the null point a deviation can be detected.
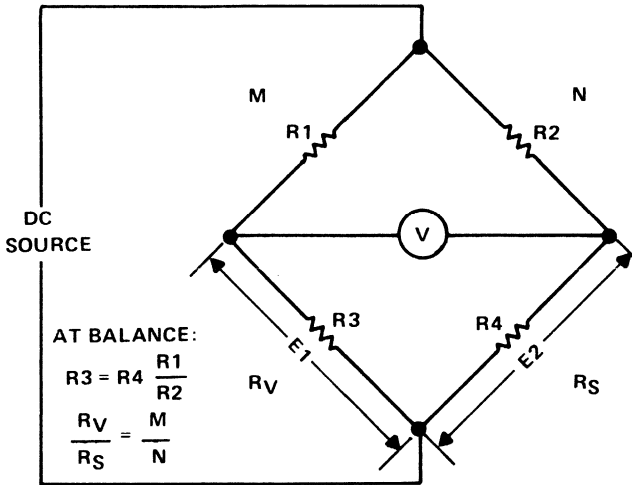
Fig. 3–2   Wheatstone Bridge Circuit.

Detecting small variations near the null point is difficult with the basic Wheatstone bridge alone. Amplification of voltage differences near the null point will improve circuit accuracy and ease of use. The bridge-balance indicator circuit (Figure 3–3) replaces the meter shown in Figure 3–2 and provides the gain required near the null-point for improved accuracy. An OP-07 operational amplifier is used as the gain element in this circuit.
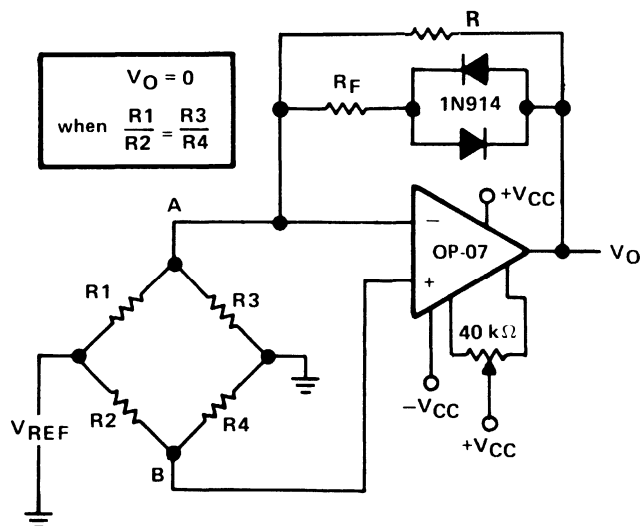
Fig. 3-3   Bridge-Balance Indicator Circuit.

In this application, the 1N914 diodes in the feedback loop result in high sensitivity near the point of balance (R1/R2 = R3/R4). When the bridge is unbalanced the amplifier's closed-loop gain is approximately R_F/r, where r is the parallel equivalent of R1 and R3. During an unbalanced condition the voltage at point A is different from that at point B. This difference voltage (V_{AB}), amplified by the gain factor G, appears as an output voltage. As the bridge approaches a balanced condition (R1/R2 = R3/R4), V_{AB} approaches zero. As V_{AB} approaches
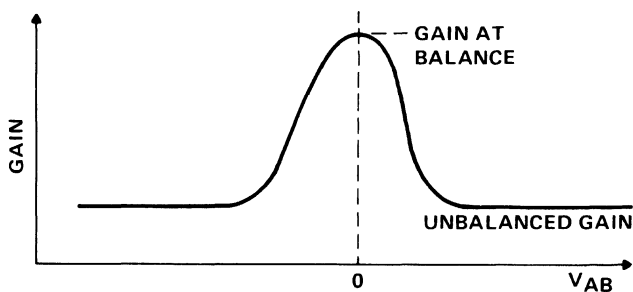
Fig. 3-4   Gain as a Function of V_{AB}.

zero the 1N914 diodes in the feedback loop lose their forward bias and their resistance increases, causing the total feedback resistance to increase. This increases circuit gain and accuracy in detecting a balanced condition. Resistor R limits the circuits maximum gain. Figure 3–4 shows the effect of approaching balance on circuit gain. The visual indicator used at the output of the OP-07 could be a sensitive voltmeter or oscilloscope.

High-Input-Impedance Differential Amplifier

One of the most useful applications of an operational amplifier is the differential-input dc amplifier configuration shown in Figure 3–5.
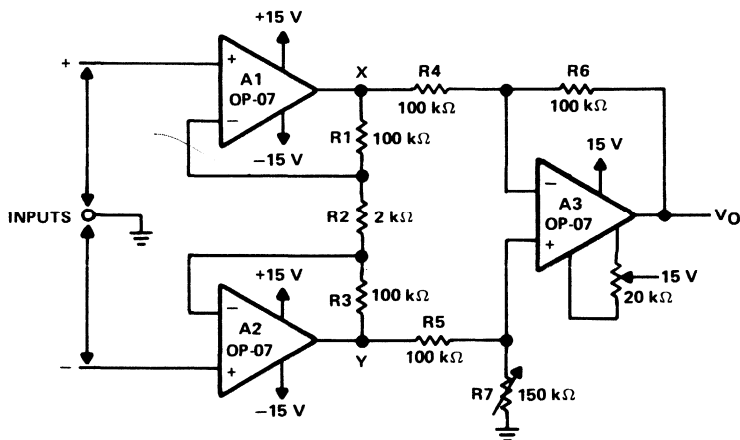
Fig. 3–5   High-Input-Impedance Differential Amplifier.

Operational amplifiers A1 and A2 are connected in a noninverting configuration with their outputs driving amplifier A3. Operational amplifier A3 could be called a subtractor circuit which converts the differential signal floating between points X and Y into a single-ended output voltage. Although not mandatory, amplifier A3 is usually operated at unity gain and R4, R5, R6 and R7 are all equal.

The common-mode-rejection of amplifier A3 is a function of how closely the ratio R4:R5 matches the ratio R6:R7. For example, when using resistors with 0.1% tolerance, common-mode rejection is greater

than 60 dB. Additional improvement can be attained by using a potentiometer (slightly higher in value than R6) for R7. The potentiometer can be adjusted for the best common-mode rejection. Input amplifiers A1 and A2 will have some differential gain but the common-mode input voltages will experience only unity gain. These voltages will not appear as differential signals at the input of amplifier A3 because, when they appear at equal levels on both ends of resistor R2, they are effectively cancelled.

This type of low-level differential amplifier finds widespread use with dc and low-frequency signals commonly received from a transducer or thermocouple output, which are amplified and transmitted in a single-ended mode. The amplifier is powered by ±15 V supplies. It is only necessary to null the input offset voltage of the output amplifier A3.

Low Voltage Shunt Limiter

In some circuits, it is necessary to symmetrically limit or clip the peak output voltage of an amplifier stage. Limiting may be required to prevent overdriving a following amplifier stage. This type of circuit is also used in volume compressor and amplitude leveler designs.

The limiting function may be accomplished by several methods. Figure 3–6 shows a simple back-to-back diode limiter.
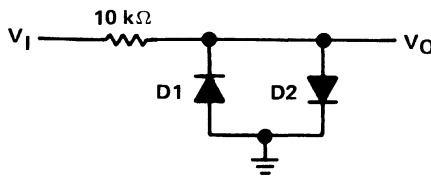
Fig. 3–6   Simple Back-to-Back Shunt Limiter.

If standard small signal diodes such as 1N914 are used for D1 and D2, ±0.6 V would be available at the limiter output. If germanium diodes are used for D1 and D2, ±0.3 V will be the output voltage. Limiting may also be accomplished utilizing resistor/zener diode networks. The low-voltage shunt limiter shown in Figure 3–7 is useful when the signal level must be limited at a very low level, such as several

hundred millivolts. Such levels are, of course, below the range of conventional diodes, so alternative methods are necessary to accomplish limiting at these levels.
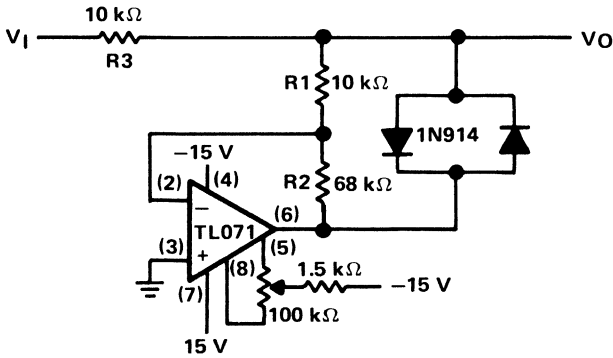
Fig. 3–7   Low-Voltage Shunt Limiter.
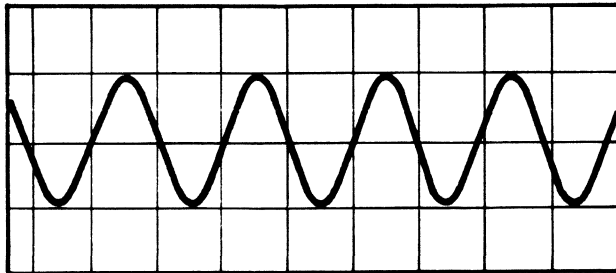
10-VOLT PEAK-TO-PEAK INPUT VOLTAGE
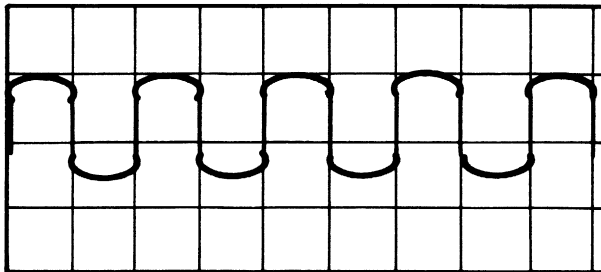
150-mV PEAK-TO-PEAK OUTPUT VOLTAGE

Fig. 3–8   Input/Output Voltage Waveforms of Low-Voltage Shunt Limiter.

In this circuit, the operational amplifier is used to shift the apparent threshold of a conventional 1N914 silicon diode. The output voltage limit can be adjusted to any fraction of the diode voltage. This circuit divides the signal level, even when below the threshold, because of the feedback through resistor R2. As an example, assume a 10 V peak-to-peak input sine-wave signal at a frequency of 1 kHz. With the values shown the output will be a 150 mV peak-to-peak square wave as shown in the scope photos in Figure 3–8.

PTC Thermistor Automotive Temperature Indicator

To reach maximum efficiency, present day automobiles require many control methods. For example, temperature control of engine parts and fluids is essential. However, accurate electronic temperature measurements are not simple. Of the variety of thermocouples, resistance sensors, and thermistors available, the positive-temperature-coefficient silicon thermistor is an excellent choice for this application. Planar technology using the spreading-resistance principle allows this integrated circuit to be built. The TSP102 has a positive resistance
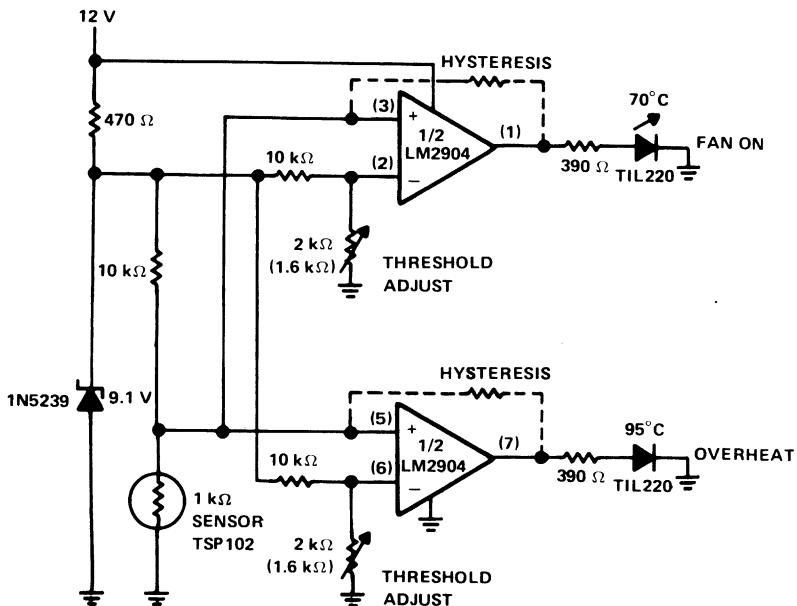
Fig. 3–9   PTC Sensor Automotive Temperature Control Circuit.

temperature coefficient of 0.7%/°C and has very close resistance tracking from unit to unit. Nominally it is about 1 kΩ resistance at 25°C and changes from 545 Ω at −40°C to 1665 Ω at 120°C.

The example circuit (Figure 3–9) is used to indicate two different water temperature trip points by turning on LEDs when the temperatures are reached. The circuit is constructed around the LM2904 dual operational amplifier which was designed mainly for the automotive industry.

The circuit is powered from the 12 V auto system. The 1N5239 zener diode supplies a regulated 9.1 V to give stable reference voltages for the circuit. The thermistor is in series with a 10 kΩ resistor from ground to the positive 9.1 V point. The top of the thermistor is tied to both noninverting inputs of the LM2904. The voltage at these inputs will change as the thermistor resistance changes with temperature. Each inverting input on the LM2904 has a reference, or threshold trip point, set by a 10 kΩ resistor and a 2 kΩ potentiometer in series across the 9.1 V regulated voltage. When this threshold is exceeded on the noninverting input of LM2904, the TIL220 LED lights. In this circuit, the FAN ON trip point was set at 70°C. This occurs with approximately 1.3 V on the inverting input of the top section of the LM2904. The OVERHEAT trip point was set at 95°C. This condition exists when the bottom section of the LM2904 has approximately 1.44 V on the inverting input. The two trip points can be recalibrated or set to trip at different temperatures by adjusting the 2 kΩ potentiometer in each section. In addition to being used as warning lights as shown here, circuits can be added to turn on the fan motor or activate a relay.

Other types of thermistors and temperature sensors manufactured by other companies can be used with this type of circuit.

Stable 10 Volt Reference

A stable 10 V reference is a valuable asset for calibrating oscilloscopes and other laboratory equipment. The 10 V reference was selected because it can be used in decade fashion (multiplied or divided by 10). One of the major requirements for a laboratory reference is not only initial accuracy but long-term stability. This requires precision low-drift components. An OP-07 bipolar operational amplifier was chosen because it has low offset and long-term stability. The offset

voltage drift is approximately 0.3 μV/°C. The OP-07 is excellent because of its low noise and high-accuracy amplification of very low-level signals. Figure 3–10 illustrates an accurate 10 V reference circuit.
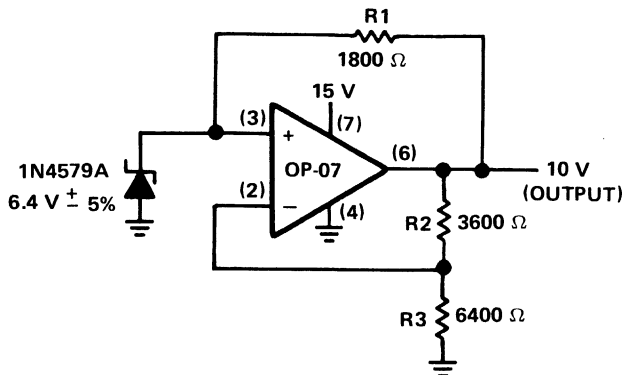
Fig. 3–10   Accurate 10 Volt Reference Circuit.

The accuracy of the circuit can be enhanced by using precision resistors. The 1N4579A zener diode was chosen because of its 0.0005%/°C temperature coefficient. The resistor values were calculated from the following formulae:

$$R1 = \frac{10 \text{ V} - V_Z}{2 \times 10^{-3}}$$

Where:

V_Z = Zener Voltage

$$R2 = \frac{10 \text{ V} - V_Z}{1 \times 10^{-3}}$$

$$R3 = \frac{V_Z}{1 \times 10^{-3}}$$

Assuming a zener diode voltage of 6.4 V, resistors R2 and R3 total 10 kΩ from the 10 V output to ground. The values of R2 and R3 are calculated to have 6.4 V between their junction and ground. This voltage is applied to the inverting input of the OP-07. Resistor R1 has

0.002 A of current and a 3.6 V drop across it, hence a value of 1800 Ω. This establishes a stable reference at the noninverting input of the OP-07. If the output voltage moves either higher or lower, the operational amplifier holds it at 10 V. By using the recommended components good long-term stability at the desired output voltage can be expected. If other voltages are needed, they can be calculated with the same formulae. However, the output voltage can never be lower than the reference zener diode voltage. To compensate for zener and other component variations, a multiturn potentiometer may be used at the junction of R2 and R3.

Precision Large-Signal Voltage Buffer Using an OP-07

The primary purpose of the voltage-follower circuit is to buffer an input signal from its load.

The circuit in Figure 3–11 is a precision large-signal voltage buffer with a worst-case accuracy of 0.005%. This accuracy is possible because of the ultralow input-offset voltage of the OP-07. With ±15 V power supplies, an input signal with a ±14 V swing can be used. Under these conditions, a peak-to-peak output voltage swing of ±13 V can be expected. The OP-07 is an extremely stable device for use in this type of circuit.
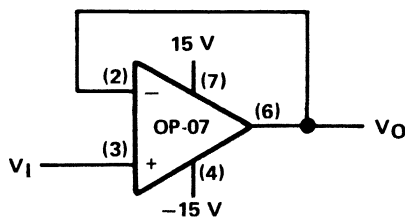
Fig. 3–11   Precision Large-Signal Voltage Follower.

ACTIVE FILTER APPLICATIONS

Introduction

Active filters, by the use of resistors, capacitors and operational amplifiers, allow the realisation of filters with the transfer function

characteristics of passive filters constructed with inductors, capacitors and resistors. Advantages of active filters include low output impedance, cascaded stages without gain loss, and the capability of generating filtering functions having relatively high Q at low frequencies without inductors.

Depending on the circuit type: low-pass, high-pass, band-pass, or band-reject filters can be designed with a roll-off characteristic from 6 to 50 dB or greater per octave. An active filter offers several advantages over a passive (LC) filter.

1. No insertion loss. The op-amp can provide gain if needed.

2. Cost. Active filter components are more economical than inductors.

3. Tuning. Active filters are easily tuned and adjusted over a wide range without altering the desired response.

4. Isolation. Active filters have good isolation due to their high input impedance and low output impedance, assuring minimal interaction between the filter and its load.
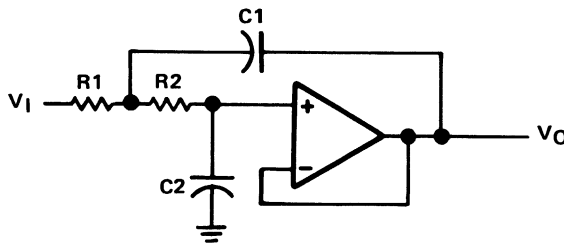
(a) LOW-PASS FILTER
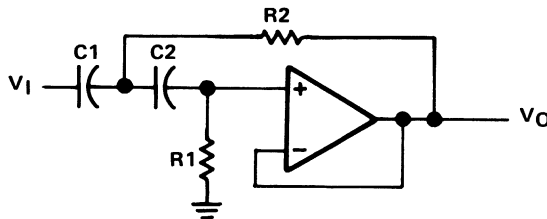
(b) HIGH-PASS FILTER

Fig. 3–12   High-Pass and Low-Pass Filter Circuits.

High- and Low-Pass Active Filters

Unity-Gain Active Filters

The unity-gain active filter is the simplest to design. It combines an operational amplifier connected in a unity gain configuration with RC filter networks. It can be either a low-pass filter [Figure 3–12(a)], or a high-pass filter [Figure 3–12(b)], depending upon the positions of its discrete resistors and capacitors.

The -3 dB (cutoff) frequency of the filter can be determined from the following equations:

Low-frequency cutoff $f_o = \dfrac{1}{2\pi\, C2\sqrt{R1R2}}$

High-frequency cutoff $f_o = \dfrac{1}{2\pi\, R2\sqrt{C1C2}}$

The Q of the circuit can be calculated using the following formulae for a low or high pass filter:

Low-pass filter $Q = 1/2\sqrt{C1C2}$

High-pass filter $Q = 1/2\sqrt{R1R2}$

These formulae are valid for a value of Q greater than 10.

Low-Pass Active Filters

Figure 3–13 illustrates the response curve typical of a second order low-pass active filter using a general-purpose operational amplifier. Outside the passband, the attenuation is computed at 12 dB per octave. However, at high frequencies the attenuation of the filter is less than predicted. In simple theory, the operational amplifier is considered to be perfect, and, for a typical general-purpose operational amplifier, this perfection proves to be acceptable up to 100 kHz. However, above 100 kHz the reduction in loop gain can no longer be ignored. The effect of this factor causes a loss of attenuation at high frequencies. General-purpose operational amplifiers are most effective in the audio frequency range. For higher frequency applications, a broad band amplifier such as the LM318 or TL291 should be used.
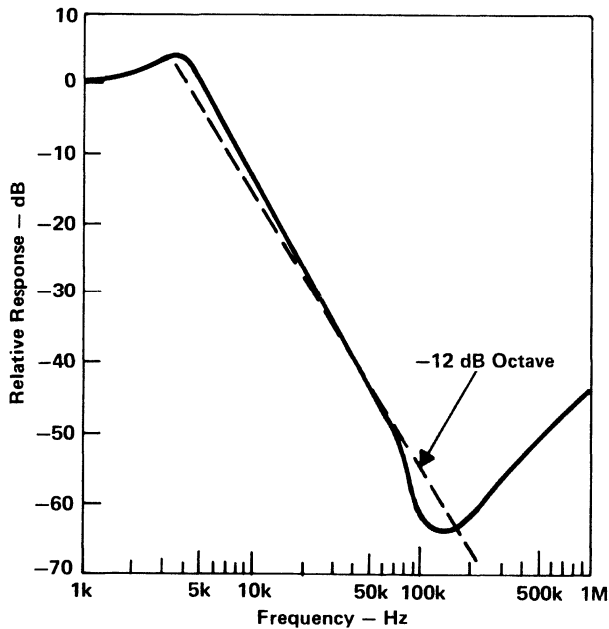
Fig. 3–13   Response Curve of a Low-Pass Active Filter.

When the frequency spectrum of the input signal is especially wide, the high-frequency rejection characteristic must be considered. The high-frequency-cutoff problem can be resolved by using a simple RC filter ahead of the active filter. The combination of an RC filter and an active filter having superior low-frequency performance will significantly improve high-frequency cutoff. In addition, an impedance adapter should be inserted between the two filters shown in Figure 3–14.

Butterworth High- and Low-Pass Filters

Among the many types of filter circuits, the 'Butterworth' filter is often the best overall choice because it has a 'maximally' flat passband and reasonable overshoot. It also has a characteristic that sets all cascaded sections to the same frequency, which makes voltage control and wide-range tuning easier. Complex filters are normally built using first and second-order networks. A first-order section is not very useful by itself as a filter because all you can control is the cutoff and impedance level. In a second-order section, it is possible to control the impedance level, the cutoff and another feature called damping, or its inverse, Q. Damping, or Q, sets the peaking or drop of the response near the cutoff frequency.
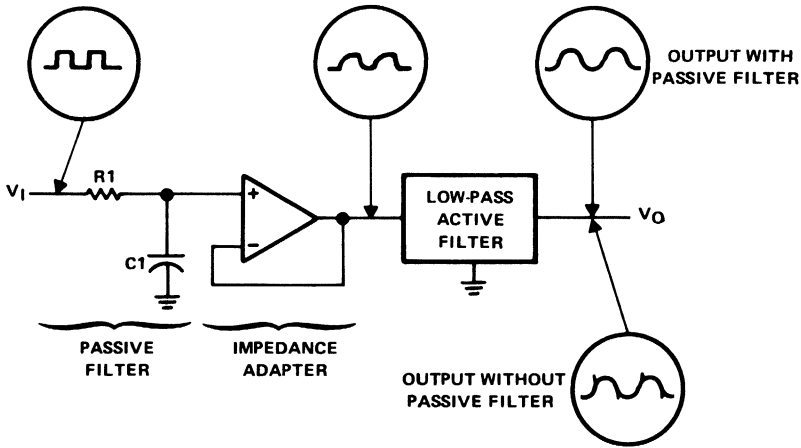
Fig. 3–14   Use of a Passive Filter Preceding an Active Filter.

The simplest second-order low-pass filter is the voltage-controlled-voltage-source (VCVS) circuit shown in Figure 3–15. In this circuit the capacitors have very little effect at low frequencies, which results in an essentially flat low frequency response. At high frequencies the capacitors separately shunt the signal to low-impedance points, one to ground and one to the output. This two-step shunting causes the response at high frequencies to fall off as the square of the frequency; hence the name, second-order section. The performance starts out flat at low frequencies and falls at 12 dB/octave, or 40 dB/decade past the cutoff frequency.
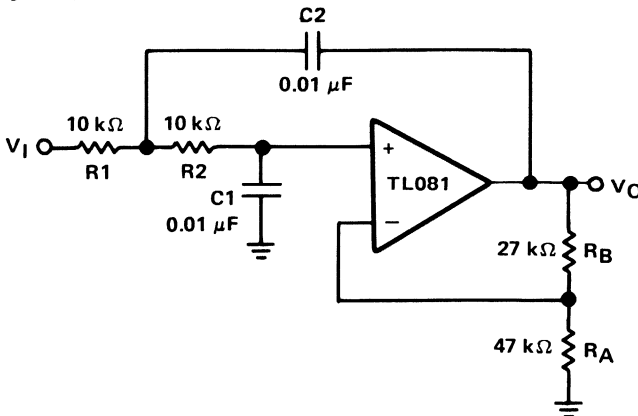
Fig. 3–15   Second Order Low-Pass Filter.

The most common approach for selecting the values of the two resistors and capacitors in the filter section is to make R1 and R2 equal, and C1 and C2 equal. The cutoff frequency is simply:

$$f_o = \frac{1}{2\pi RC}$$

This is called an 'equal-component' low-pass filter. The passband gain is fixed at 1.586 (+4 dB) for a second-order Butterworth response, and is the only gain that will permit this circuit to function properly. The cutoff point will be 3 dB from the passband gain of +4 dB, +1 dB.

Since the op-amp is in the noninverting mode, the feedback resistor R_B must be 0.586 times the value of the input resistor R_A for a voltage gain of 1.586. To build a low-pass Butterworth filter with a cutoff frequency of 1500 Hz you choose the component values in the following manner. Let $R_A = 47$ kΩ. R_B would be $R_A \times 0.586$ or about 27 kΩ. If we let the capacitor value be 0.01 μF, the resistors will be selected by the formula:

$$R1 = \frac{1}{2\pi f_o C}$$

$$= \frac{1}{(6.28)\,(1500)\,(0.01 \times 10^{-6})}$$

$$= 10{,}617\ \Omega = R2$$

The nearest standard value would be 10 kΩ.
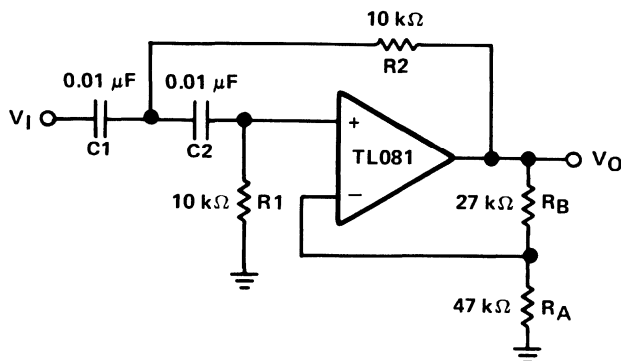
Fig. 3–16   Second Order High-Pass Filter.

Simply interchanging the position of the resistors and capacitors as shown in Figure 3–16 produces a high-pass active filter with the same cutoff frequency. The passband gain is also 1.586, or +4 dB. Figure 3–17 shows the response curves of both of these filters.
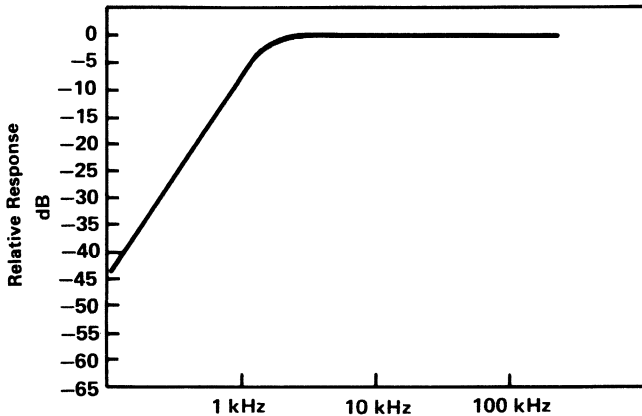
(a) HIGH PASS
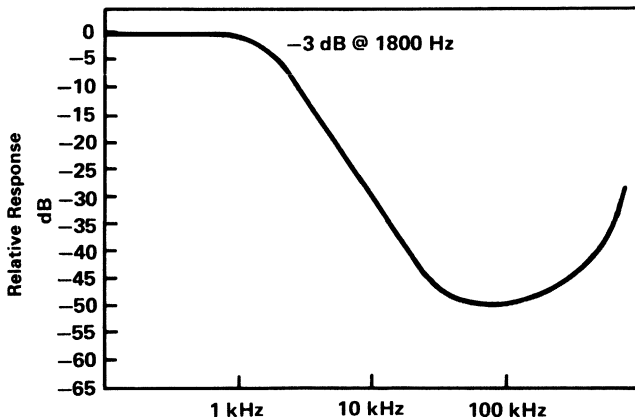
(b) LOW PASS

Fig. 3–17   Active Filter Response.

Bandpass Active Filters

A bandpass filter permits a range of frequencies to pass while attenuating frequencies above and below this range. The centre

frequency (f_o) is the frequency at which the maximum voltage gain occurs. The bandwidth of this type of filter is the difference between the upper and lower frequencies at the points where the voltage gain is 0.707 times the maximum value, or 3 dB lower than the response at the centre frequency. As shown in Figure 3–18, f_L is called the lower 3 dB frequency and f_H is called the upper 3 dB frequency. Bandwidth is determined by the following equation:

Bandwidth = $f_H - f_L$

The bandpass filter bandwidth and centre frequency are related to each other by the Q, which is defined as follows:

$$Q = \frac{f_o}{f_H - f_L} \text{ or } \frac{f_o}{BW}$$

Bandpass filter responses like those shown in Figure 3–18 can be built with operational amplifiers.
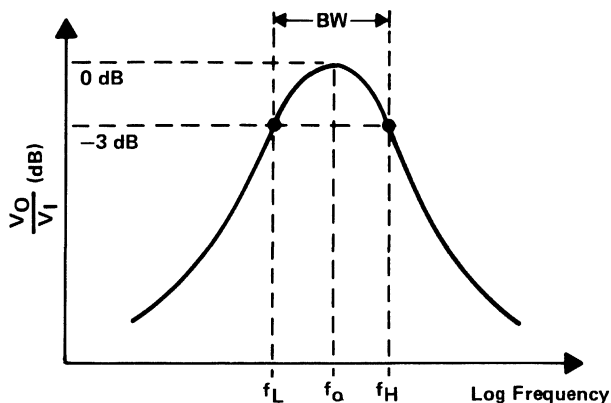
Fig. 3–18   Bandpass Filter Response Curve.

Multiple-Feedback Bandpass Filters

The basic multiple-feedback band-pass filter is useful for Qs up to about 15 with 'moderate' gain. Bandpass circuits normally have lower damping and higher Q values than the usual low-pass or high-pass

responses. In fact, these circuits are progressively harder to build and tune as the damping goes down and the Q goes up. Experience has shown that a high-performance, high-Q bandpass active filter cannot be built with a single op-amp. Component-tolerance problems, sensitivity problems, or severe gain restrictions provide unsurmountable barriers as you try to increase the circuit Q of single op-amp circuits beyond a certain point. Therefore, single op-amp versions of this filter may be used only for low-Q applications (Qs in the 2 to 5 range). Fortunately, Q values of 2 to 5 are ideal for many audio applications, including equalizers and tone controls. Higher Q circuits find use at IF and RF frequencies.

Figure 3–19 shows a single-stage, multiple-feedback bandpass filter where the op-amp is connected in the inverting mode. Resistor R3 from the output to the inverting input sets the gain and the current through the frequency-determining capacitor, C1. Capacitor C2 provides feedback from the output to the junction of R1 and R2. C1 and C2 are always equal in value. Resistor R2 may be made adjustable in order to adjust the centre frequency which is determined from:

$$f_o = \frac{1}{2\pi C} \left[\frac{1}{R3} \times \frac{R1 + R2}{R1R2} \right]^{1/2}$$
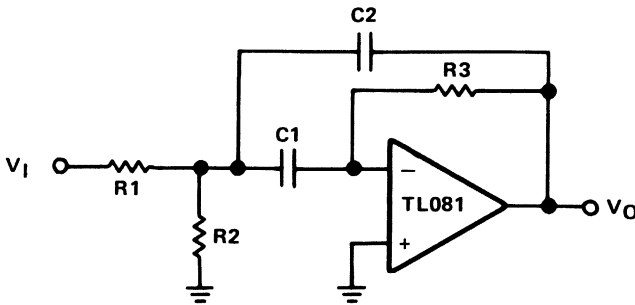
Fig. 3–19   Single Stage Feedback Bandpass Filter.

When designing a filter of this type it is best to select a value for C1 and C2, keeping them equal. Typical audio filters have capacitor values from 0.01 μF to 0.1 μF which will result in reasonable values for the resistors. We will design a filter for 10 kHz and assume a Q of 3 and a

stage gain of 2. The three resistor values are then determined from the following equations:

$$R1 = \frac{Q}{2\pi fCG} = 2388.5$$

or 2.4 kΩ (nearest standard value)

$$R2 = \frac{Q}{2\pi fC\,(2Q^2 - G)} = 298.5$$

= or 300 Ω (nearest standard value)

$$R3 = \frac{Q}{\pi fC} = 9554$$

or 10 kΩ (nearest standard value)

Where

G = 2

Q = 3

C = 0.01 μF

f = 10 kHz

As previously stated, a single-stage active filter of this type results in low Qs (2 to 5). Filters which provide a very narrow passband must have a much higher Q than possible with a single section using one op-amp. This may be achieved by using several cascaded stages. Another method to achieve higher Q is the use of positive feedback. Figure 3–20 shows a positive-feedback bandpass filter using four op-amps which make up two sections.
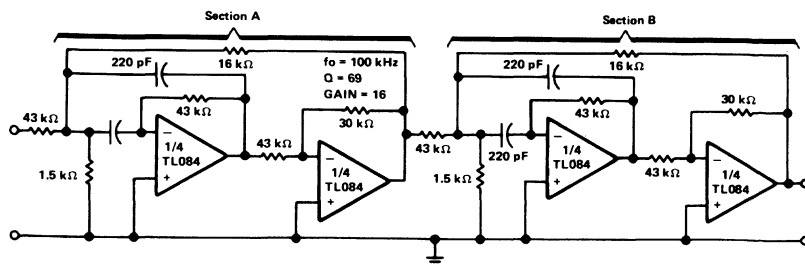
Fig. 3–20   Positive Feedback Band-Pass Filter.

The complete filter is comprised of two identical sections, section 'A' and section 'B'. Each section uses an op-amp connected as a multiple-feedback bandpass filter and a second op-amp used as a phase inverter to apply positive feedback to the input of the first op-amp. This allows section Q's of up to 50 with reduced Q sensitivity to circuit tolerances. The overall gain of section 'A' is 4.

When section B is cascaded to section A we have the complete two stage (4 op-amp) filter with an overall gain of 16 and Q of 69. The scope photo in Figure 3–21 shows the bandwidth of both stages cascaded. The measured bandwidth with an f_o of 100 kHz is 2.3 kHz at the −3 dB or half-power points.
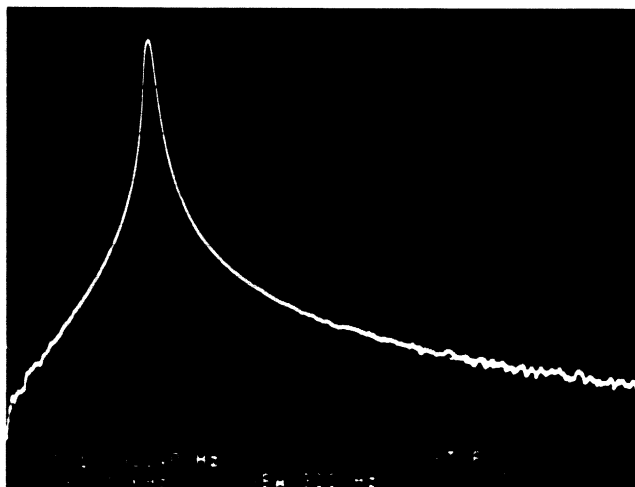
Fig. 3–21   Band-Pass Filter Response.

Twin-T Notch Filter

A notch filter is used to reject or block a frequency or band of frequencies. These filters are often designed into audio and instrumentation systems to eliminate a single frequency, such as 60 Hz. Perhaps the best-known passive notch filter is the 'twin-T' filter. The circuit is shown in Figure 3–22.
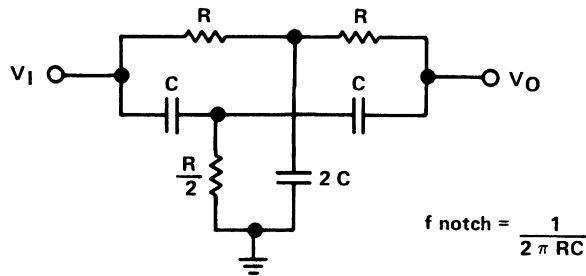
Fig. 3–22   Twin-T Notch Filter.

If the six components are carefully matched, theoretically you can obtain an almost infinite rejection at the null frequency. Commercial grade components (5%–10% tolerance) produce a null depth of at least 30 to 40 dB.
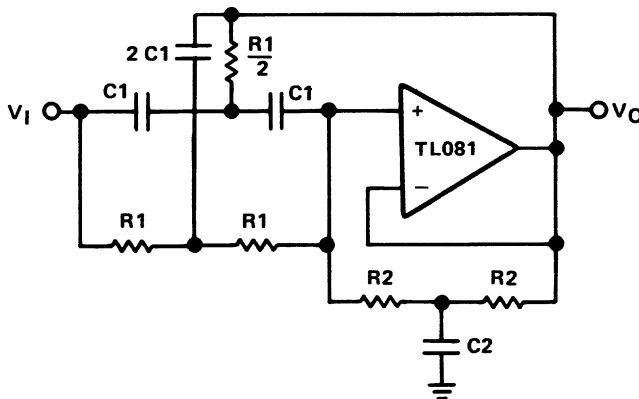
Fig. 3–23   Active Twin-T Notch Filter.

When this twin-T network is combined with a TL081 op-amp in a circuit, an active filter can be implemented as shown in Figure 3–23. Notice the added resistor capacitor network (R2, C2), effectively in parallel with the original twin-T network, on the input of the filter. These networks set the Q of the filter. The op-amp is basically connected as a unity-gain voltage follower. The Q is found from:

$$Q = \frac{R2}{2R1} = \frac{C1}{C2}$$

Let's now design a 60 Hz notch filter with a Q of 5 using the circuit in Figure 3–23. It is usually best to pick the C1 capacitor value and calculate the resistor R1. Let C1 = 0.22 μF.

$$fn = \frac{1}{2\pi RC}$$

$$R = \frac{1}{2\pi fnC} = \frac{1}{(6.28)\,(60)\,(0.22 \times 10^{-6})}$$

R1 = 12,063 or 12 kΩ

Next calculate R2 in the Q network.

$$Q = \frac{R2}{2R1}$$

R2 = Q × 2R1 = 5 × 24 kΩ = 120 kΩ

R2 = 120 kΩ

Finally, calculate C2 from the equation.

$$Q = \frac{C1}{C2}$$

$$C2 = \frac{C1}{Q} = \frac{0.22\,\mu F}{5} = 0.044\,\mu F$$

C2 = 0.047 μF (nearest standard value)

Standard 5% resistors and 10% capacitors produce a notch depth of about 40 dB as shown in the frequency response curve (Figure 3–24).
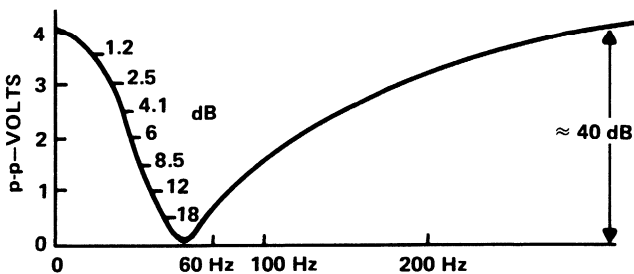
Fig. 3–24   60 Hz Twin-T Notch Filter Response.

AUDIO OP-AMP APPLICATIONS

Mike Preamp with Tone Control

Microphones may be classified into two groups: high-impedance (≈ 200 kΩ) with high-voltage output and low-impedance (≈ 200 Ω) with low-voltage output. The output from a high-impedance microphone can be amplified simply and effectively with a standard inverting or noninverting operational amplifier configuration. However, high-impedance microphones are more susceptible to stray RF and 60 Hz noise. They have a fairly flat frequency response but are usually restricted to short cable lengths (10 feet or less). Long cables result in a high frequency roll-off characteristic caused by the cable capacitance.

Low-impedance microphones also have a flat frequency response but their low output levels impose rather stringent noise requirements on the preamp. The preamp shown in Figure 3–25 operates from a low-impedance, unbalanced, two-wire microphone where one of the wires is ground. The circuit consists of the LM318 preamp and the tone control circuitry.
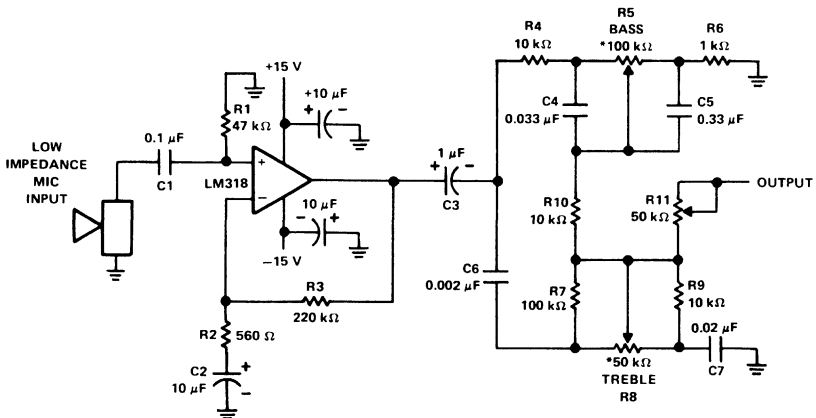
*THE TONE CONTROLS ARE AUDIO TAPER (LOG) POTENTIOMETERS.

Fig. 3–25   Mike Preamp With Tone Control.

The LM318 op-amp is operated as a standard noninverting amplifier. Resistor R1 (47 kΩ) provides an input path to ground for the bias current of the noninverting input. The combination of R2 (560 Ω)

and C2 (10 μF) provide a frequency roll-off below 30 Hz. At 30 Hz and above the gain is relatively flat at about 50 dB, set by the ratio R3/R2. R3 (220 kΩ) provides negative feedback from the output to the inverting input of the op-amp. C3 (1.0 μF electrolytic) ac couples the preamp to the tone control section.

The top half of the tone control section is the bass control. The bottom half controls the treble frequency response. These tone controls (R5 and R8) require audio taper (logarithmic) potentiometers. The 50 kΩ potentiometer on the output can be used to set the output or gain of the preamp. Figure 3–26 shows the bass and treble responses of the circuit.
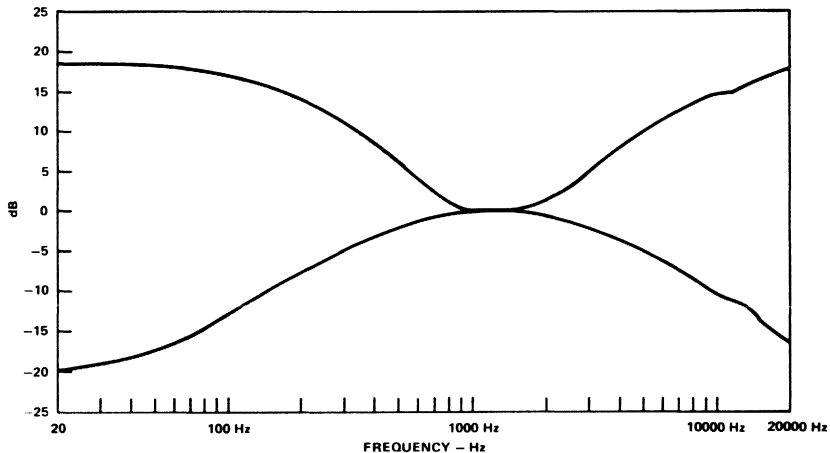
Fig. 3–26   Preamp Frequency Response.

TL080 IC Preamplifier

A preamplifier is needed to amplify the signal generated by a tape head or phonograph cartridge. It is also common to include, with the preamplifier, a means of altering the bass and treble frequency response. The 'purist' may want the amplifier to be 'flat', which means no change from the input's frequency response. This condition should occur with both bass and treble controls at midposition. Sometimes it may be necessary to compensate for the effects of room acoustics, speaker response, etc. Also there is simply a matter of personal taste; one person may prefer music with heavier bass; another may prefer stronger treble.

Active tone control circuits offer some advantages: they are inherently symmetrical in boost and cut operation and have very low total harmonic distortion (THD) because they are incorporated in the negative feedback loop.
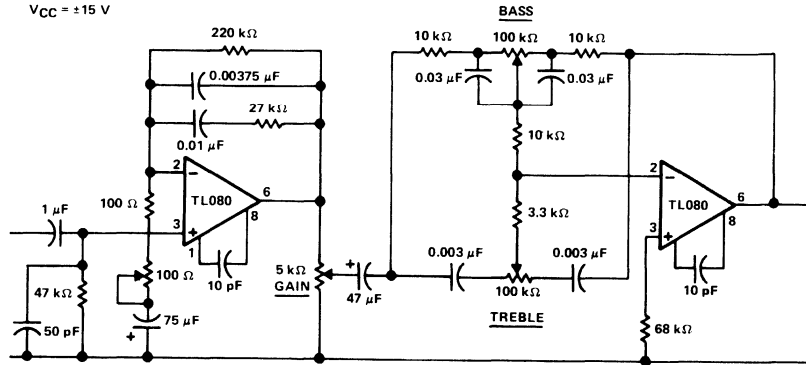
Fig. 3–27   IC Preamplifier.

The circuit shown in Figure 3–27, is a form of the so-called 'Americanised' version of the Baxandall negative-feedback tone control. At very low frequencies the reactance of the capacitors is large enough that they may be considered open circuits, and the gain is controlled by the bass potentiometer. At low to middle frequencies the reactance of the 0.03 μF capacitors decreases at the rate of 6 dB/octave, and is in parallel with the 100 kΩ bass potentiometer; so the effective impedance is reduced correspondingly, thereby reducing the gain. This process continues until the 10 kΩ resistors, which are in series with the bass pot, become dominant and the gain levels off at unity. The action of the treble circuit is similar and becomes effective when the reactance of the 0.003 μF capacitors becomes minimal. This complete tone control is in the negative feedback loop of the second TL080. Figure 3–28 shows the bass and treble tone control response. The response curves were run with 1.0 V equal to '0' dB as the 'flat' response line.

The first TL080 is a preamp with a 100 Ω adjustable gain change pot. This gives a gain adjustment of about 6 dB for matching to the output of a particular pick-up or tape head. The negative feedback loop of this TL080 contains the gain setting and frequency compensation
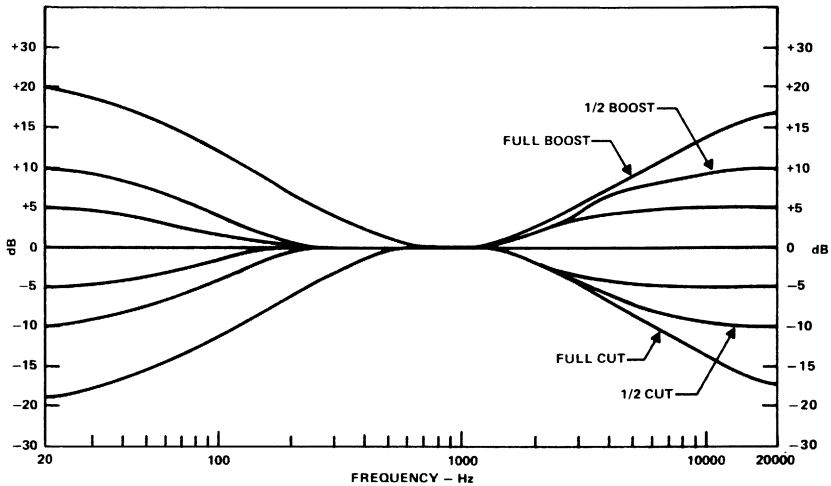
Fig. 3–28   Bass and Treble Tone Control Response.

components, which need to be optimised for the respective signal source.

Audio Distribution Amplifier

Sometimes there is a need for a preamplifier to receive the output from a single audio input device such as a microphone and drive several audio power amplifiers. This could be done most easily with a shielded cable to each amplifier from the originating preamplifier. However, if this were done by simply paralleling the shielded cables and connecting them to the preamp, the result could be an oscillating preamp stage or degraded high-frequency response due to the heavy capacitance loading.

A simple solution to this problem is the three channel output distribution amplifier using the low distortion performance of the quad operational amplifier TL084 as shown in Figure 3–29. The first stage is capacitively coupled with a 1.0 μF electrolytic capacitor. The inputs are at 1/2 V_{CC} rail or 4.5 V. This makes it possible to use a single 9 V supply. A voltage gain of 10 (1 MΩ/100 kΩ) is obtained in the first stage, and the other three stages are connected as unity-gain voltage followers. Each output stage independently drives an amplifier through the 50 μF output capacitor to the 5.1 kΩ load resistor.
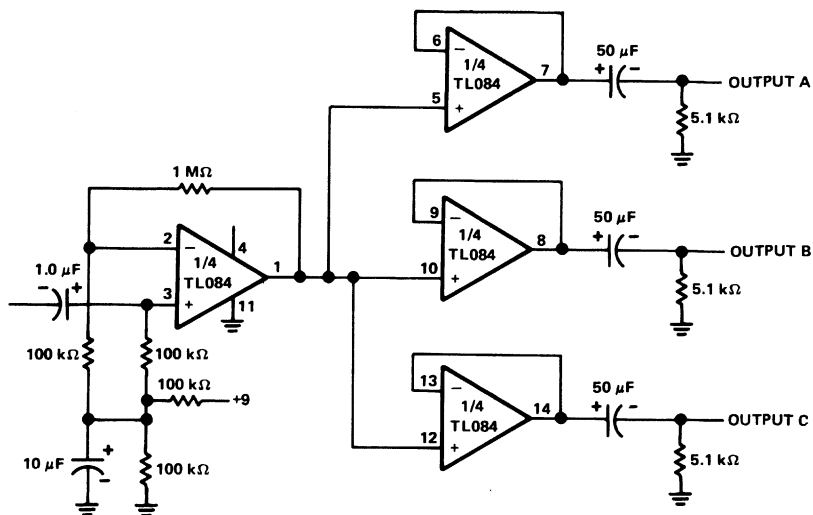
Fig. 3–29   Distribution Amplifier.

As shown in the response curve (Figure 3–30), the response is flat from 10 Hz to 30 kHz. Sinewave distortion begins at about 0.45 V_{PP} input with 5.5 V_{PP} output at 1 kHz. The total supply current is about 9 mA at maximum input of 0.45 V_{PP}. The TL070 and TL080 family of op-amps operate in true class AB and therefore offer zero crossover distortion. At a frequency of 1.0 kHz and with 3.0 V_{PP} output the total harmonic distortion is 0.14%.
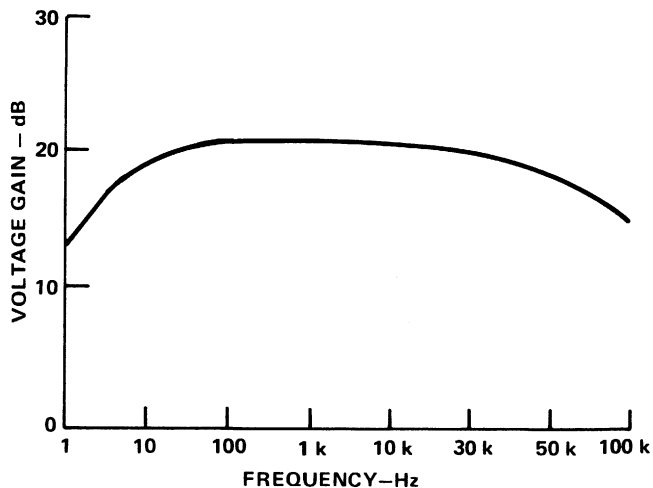
Fig. 3–30   Frequency Response Curve.

Audio Power Amplifier

Most audio amplifier circuits today are voltage output devices which apply a voltage to the terminals of the speaker. Large changes in speaker impedance with frequency yield poor frequency response with the high-frequency output falling off rapidly as the speaker impedance increases. It should be noted that the speaker cone displacement is proportional to the current in the voice coil rather than the voltage across the speaker terminals. The current is the primary mover of the voice coil.

The single speaker amplifier circuit shown in Figure 3–31 uses current feedback rather than the more popular voltage feedback. As shown, the feedback loop is from the junction of the speaker terminal and a 0.5 Ω resistor, to the inverting input of the NE5534. Sensing the current through the speaker and feeding it back provides better speaker damping than obtainable with voltage-drive systems.
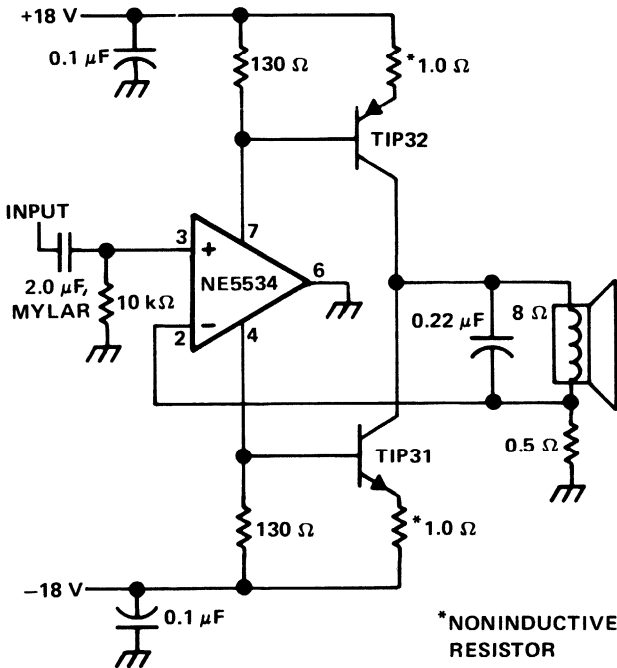
Fig. 3–31   Audio Power Amplifier.

Note the unusual grounded output pin on the NE5534 op-amp. When the input to the amplifier is positive, the power supply supplies current through the TIP32 and the load to ground. Conversely, with a negative input the TIP31 supplies current through the load to ground. The gain in this case is set to about 15 (gain = SPKR 8 Ω/0.5 Ω feedback). The 0.22 μF capacitor across the speaker rolls off its response beyond the frequencies of interest. Using the 0.22 μF capacitor specified, the amplifier output is 3 dB down at 90 kHz where the speaker impedance is about 20 Ω. The Quiescent output stage collector current is determined by the 130 Ω resistors that connect each transistor base to the appropriate supply rail, the output transistor V_{BE}, and the 1 Ω emitter resistors. To set the recommended class 'A' output collector current, adjust the value of either 130 Ω resistor. An output current of 50 to 100 mA will provide a good operating midpoint between the best crossover distortion and power dissipation.

The 0.1 μF bypass capacitors on each rail may be mylar or ceramic disk. The 2.0 μF should be a nonpolarized capacitor while the 0.22 μF across the speaker should be mylar.

Figure 3–32 shows the frequency response of the amplifier with a 2.0 μF input capacitor. This response is very flat with the −3.0 dB point on the low frequency end at 45 Hz. The −3.0 dB point at the high frequency end occurs at 80 kHz. Total Harmonic Distortion (THD) is 0.01% at 6.25 W rms output into an 8 Ω load with ±18 V on the supply rails.
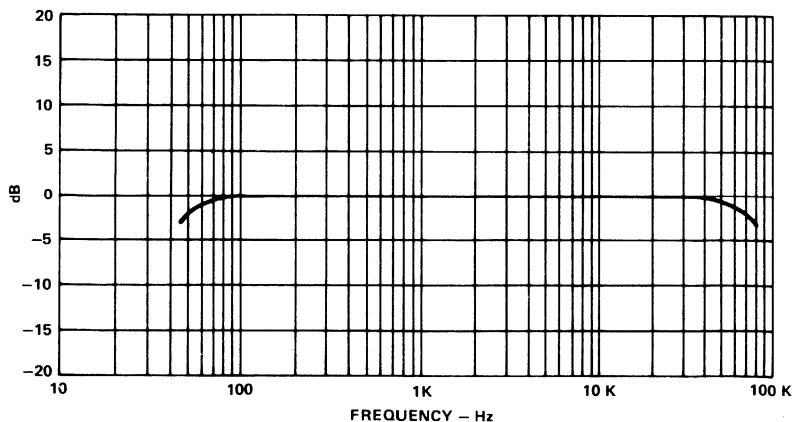
Fig. 3–32   Audio Power Amplifier Frequency Response.

This amplifier circuit uses few components, has low total harmonic distortion, excellent frequency response and is easily duplicated. It works well up to 12 W peak output before clipping is noted. The TIP31 and TIP32 output transistors are complementary power transistors in the TO-220 package. Both transistors are rated at 3.0 A continuous collector current.

OSCILLATORS AND GENERATORS

Audio Oscillator Circuit Description

A Wein bridge oscillator can be used to produce sinewaves with very low distortion level. The Wein bridge oscillator produces zero phase shift at only one frequency ($f = 1/2 \, \pi RC$) which will be the oscillation frequency. In the configuration shown in Figure 3–33 stable oscillation can occur only if the loop gain remains at unity at the oscillation frequency.
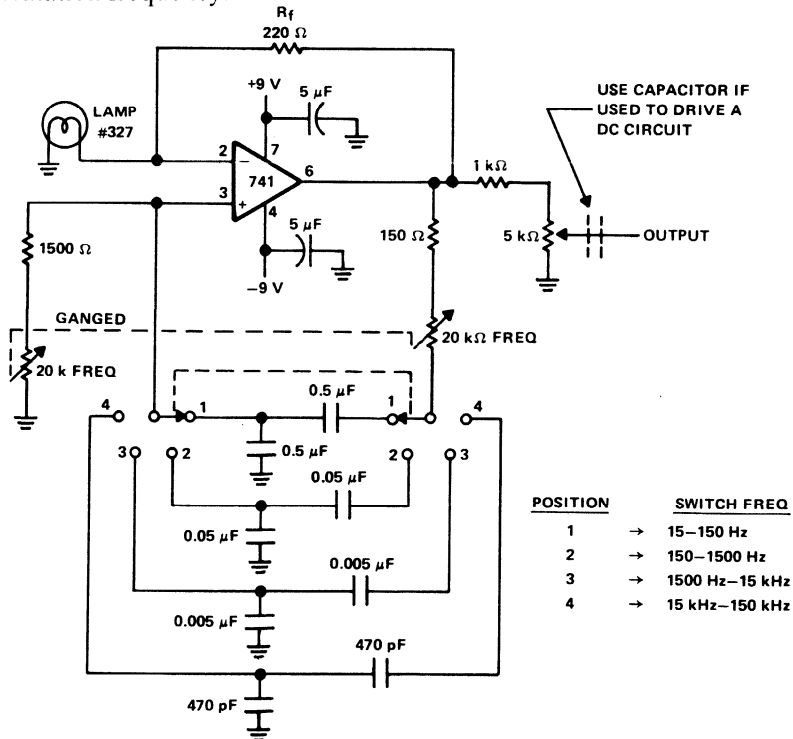
Fig. 3–33   Audio Oscillator.

The circuit achieves this control by using the positive temperature coefficient of a small lamp to regulate gain(R_f/R_{LAMP}) as the oscillator attempts to vary its output. This is a classic technique for achieving low distortion that has been used by numerous circuit designers for about 40 years. The smooth limiting action of the bulb, in combination with the Wein network's near-ideal characteristics, yields very high performance. In this circuit a 741 op-amp is used with ±9 V power supplies. The tungsten lamp is a type #327 miniature which has a standard bayonet base. This lamp is rated at 28.0 V and 40 mA. For mass production of these oscillators, the lamps are burned in for a predetermined number of hours to stabilize the characteristics of the filament.

The oscillator shown here has four frequency bands covering about 15 Hz to 150 kHz. The frequency is continuously variable within each frequency range with ganged 20 kΩ potentiometers. The oscillator draws only about 4.0 mA from the 9 V batteries. Its output is from 4 to 5 V with a 10 kΩ load and the R_f (feedback resistor) is set at about 5% below the point of clipping. As shown, the centre arm of the 5 kΩ output potentiometer is the output terminal. It should be noted that if you couple the oscillator to a dc type circuit, a capacitor should be inserted in series with the output lead.

The Basic Multivibrator

A basic multivibrator may be constructed using an operational amplifier and a few external components, as shown in Figure 3–34.

C	f
3.3 μF	0.5 Hz
0.015 μF	108 Hz
0.0015 μF	1.0 kHz
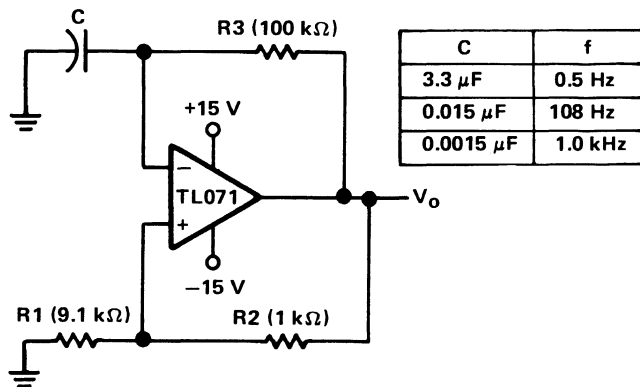
Fig. 3–34   Basic Multivibrator.

When this circuit is turned on, the natural offset of the devices serves as an automatic starting voltage. Assume the output voltage V_o goes positive and the positive feedback through R2 and R1 forces the output to saturate. The high-voltage level at V_o, then charges C through R3 until the voltage at the inverting input exceeds that at the noninverting input. As the inverting input exceeds the noninverting input level, the output switches to the negative saturation voltage. This action starts the capacitor discharging toward the new noninverting input level. When the capacitor reaches that level the op-amp switches back to the positive saturation voltage, and the process starts again.

With the TL071 the positive and negative output levels are nearly equal, resulting in a 50% duty cycle. The total time period of one cycle will be

$$t_T = 2 \ (R3)C \ \ln \ (1 \ + \ 2R1/R2)$$

LinCMOS™ OP-AMP APPLICATIONS

Microphone Preamplifier

It is sometimes necessary to have a microphone preamplifier mounted in the mike head. Obviously, the preamplifier should be as small as possible, battery operated and consume a small amount of power. In the past this was accomplished with bipolar and FET op-amps. The primary disadvantage of these circuits is the comparatively large physical size of both the amplifier and power source. Another major factor is relatively large power consumption, which requires frequent battery replacement. The LinCMOS op-amp overcomes these problems with its low power consumption and low voltage operation (down to 1.0 V).

A microphone preamplifier using a LinCMOS op-amp is illustrated in Figure 3–35. This unit comes complete with its own battery, and is small enough to be put in a small mike case. The amplifier illustrated was designed to be operated from a 1.5 V mercury cell battery at low supply currents.

This preamplifier will operate at very low power levels and maintain a reasonable frequency response as well. The TLC251
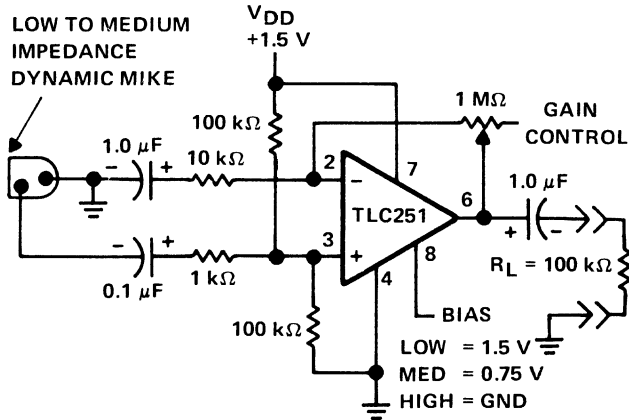
Fig. 3–35   Microphone Preamplifier.

operated in the low bias mode (operating at 1.5 V) draws a supply current of only 10 μA and has a -3 dB frequency response of 27 Hz to 4.8 kHz. With pin 8 grounded, which is designated as the high bias condition, the upper limit increases to 25 kHz. Supply current is only 30 μA under these conditions.

If improved higher frequency performance is desired, V_{DD} may be increased. For example, when using a 5 V supply the frequency response is from 27 Hz to 11 kHz for the low bias, and from 27 Hz to 220 kHz for the high bias modes respectively. Operating in the high bias mode at 5 V V_{DD} the amplifier requires a supply current of less than 500 μA.

Positive Peak Detector

Peak detectors measure and hold the maximum value of a fluctuating voltage. The purpose of the circuit in Figure 3–36 is to hold the peak of the input voltage on capacitor C1, and read the value, V_O, at the output of U2. Op-amps U1 and U2 are connected as voltage followers. When a signal is applied to V_I, C1 will charge to this same voltage through diode D1. This positive peak voltage on C1 will maintain V_O at this level until the capacitor is reset (shorted). Of course, higher positive peaks will raise this level while lower peaks will be ignored. C1 can be reset manually with a switch, or electronically with an FET that is normally off.
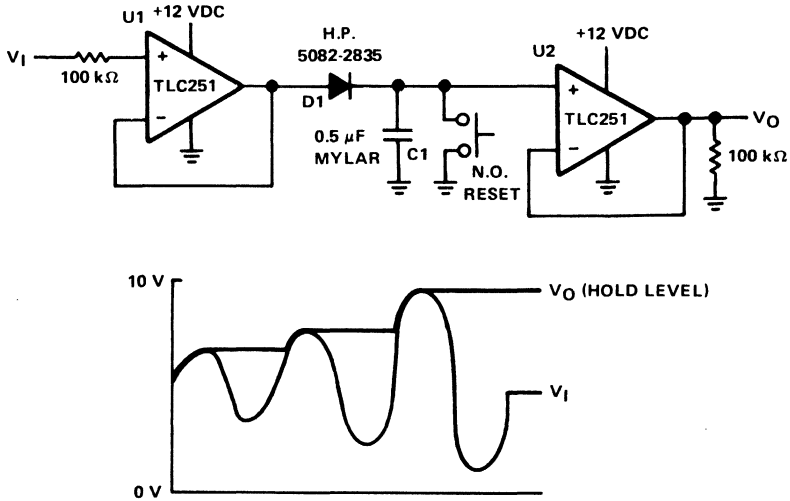
Fig. 3-36   Positive Peak Detector and Waveform.

The capacitor specified for C1 should have low leakage and low dielectric absorption. Diode D1 should also have low leakage. The op-amps selected for use in a peak detector should have high output drive and slew rate. They should also have very low input bias currents and extremely high input impedance. The TLC251 meets these requirements well. The TLC251 allows the reading of low-level signals near ground because its input-common-mode range includes the negative connection to the power supply. Peak values of negative polarity signals may be detected by reversing D1.

Instrumentation Meter Driver

Instrumentation amplifier circuitry which has incorporated low-cost general-purpose op-amps provides the designer with economical, quality performance options. Improved instrumentation amplifier circuits are possible because of the development of op-amps using junction FETs. These op-amps have improved input impedance characteristics and ac performance compared with general purpose bipolar devices. Metal gate CMOS op-amps have reduced the power required and will operate at voltages as low as 2 V.

Because the input offset voltage of a metal gate CMOS circuit changes with applied differential input voltage levels, there is a severe drawback in using this technology for op-amps. LinCMOS technology overcomes these disadvantages. LinCMOS devices do not have an input offset shift with differential input voltage and can operate satisfactorily down to 1.0 V supply. TLC271 LinCMOS op-amps are used in the instrumentation amplifier illustrated in Figure 3–37 because of their unique features. Some of these features are:

● Operate at low voltages

● Input signal operation close to −V$_{CC}$ rail

● Reasonable ac performance at low power

● Provide the high input impedance characteristic of FET input devices

● Offset stability

● High CMRR

● Power/performance adjustment for desired performance levels while maintaining the lowest possible power requirement.
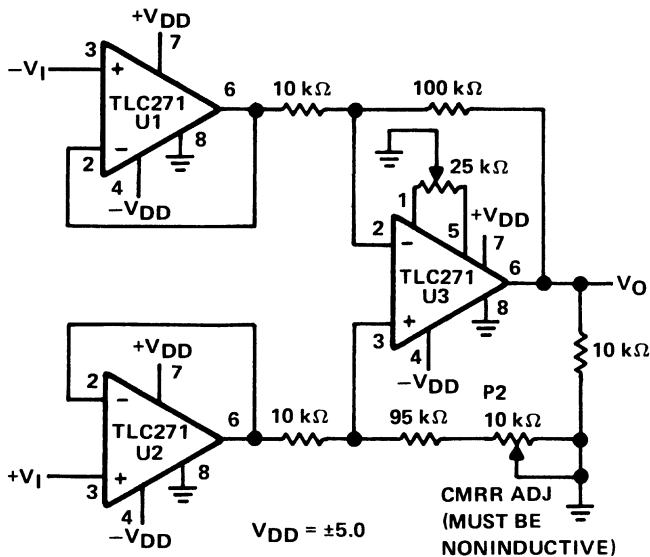
Fig. 3–37   TLC Low Power Instrumentation Amplifier.

The TLC271 operational amplifiers (the first monolithic devices to combine these characteristics) allow the construction of a ±5 V instrumentation amplifier with reasonable ac performance. Some of the important features of Figure 3–37 which should be pointed out are:

● Three op-amps U1, U2, and U3 are connected in the basic instrumentation amplifier configuration.

● Operating from ±5 V, pin 8 of each op-amp is connected directly to ground and provides the ac performance desired in this application (high bias mode).

● Two adjustment pots are used. P1 is for offset error correction and P2 allows adjustment of the input common mode rejection ratio.

● The high input impedance allows metering of signals from sources of several megohms without loading. The resulting circuit frequency response is 200 kHz at −3 dB and has a slew rate of 4.5 V/μs. This is a significant improvement over general bipolar performance. The signal response and speed characteristics are particularly significant in light of the low supply voltage and supply currents. Total supply current is 670 μA per supply.

● Output error voltages of less than 1% are experienced over the 0°C to 70°C operating range.

A Stable Two-Volt Logic Array Power Supply

The popularity of logic gate array devices has emphasized the need for closely regulated low-voltage power supplies. Typical power requirements for these devices are ±2.0 V at approximately 250 mA per array. A major requirement for many systems is the ability of the power supply to operate over a wide range of input voltages, particularly from 5 V or less to minimise losses. Regulation to within ±5% and good ripple rejection are also desirable in most applications.

Several types of three-terminal adjustable series pass regulators or shunt regulators are capable of providing regulation at 2 V. For example the LM317 will provide 2 V with a minimum number of external components. Good regulation is possible with this device when supply voltages are in excess of 5 V. LM317 operating characteristics will begin to deteriorate at 5 V or less because of insufficient input to output differential voltage.

Adjustable zeners such as the TL431 will operate at low voltage levels. However, they do not produce enough output current to be useful as a regulator in this application.
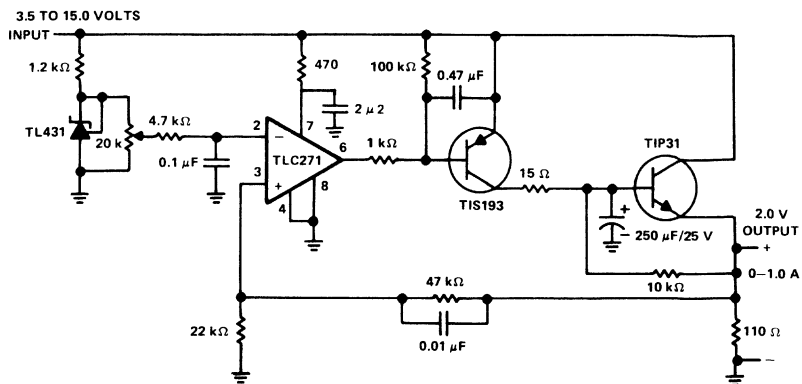
Fig. 3–38   TLC271 Logic Array Power Supply.

Combining a TL431, to provide an accurate reference; an op-amp, for accurate output level control; with a power pass transistor is very effective (Figure 3–38). However, this configuration puts some rather severe constraints on the op-amp used, as shown below:

1. It should be a device capable of operating below 5 V and handling high input, common-mode voltages (up to 2 V when operating from a single 3.5 V supply).

2. Accommodate varying differential input voltage without adversely affecting input offset stability. ˙

3. Provide adequate output drive current while maintaining a low operating current for maximum circuit efficiency.

The TLC271 is such a device.

In the application discussed here the TLC271 must operate from a single supply that can be as low as 3.5 V. A temperature compensated voltage reference is provided by the TL431 and coupled to the inverting input of the TLC271. The power supply output of 2.0 V is sensed and fed back to the TLC271's noninverting input. This results in a common-mode input level of about 2.0 V which can easily be handled by the TLC271 even when operating from a single 3.5 V supply. The TLC271's high-bias, open-loop gain of approximately 96 dB (at a V_{CC} of 3.5 V) provides control of the output drive transistors with minimum

error. Most of the no-load supply current required is drawn by the 110 Ω load shunt at the 2 V output (20 mA). The supply's total no-load current with a 15 V input is less than 30 mA.

The circuit's stability is excellent for both input voltage and output current variations. Maximum variation of output voltage, with input voltage swings from 3.5 V to 15 V, is less than 5%. Ripple rejection with a 2 V input swing at 120 Hz was over 60 dB. Variation in output voltage from no load to full load is less than 0.5%. The capability of the TLC271 to operate from a 3.5 V supply and handle 2 V common-mode input signals without input overloading coupled with the inherent input offset stability of the Silicon Gate CMOS process, makes this kind of performance possible.

TLC271 Twin-T Notch Filter

The theory of a bipolar twin-T notch filter was discussed in the section under Active Filter Applications. That twin-T filter required ±15 V power supplies. This filter however, can be powered with a single 5 V supply. Active filters built with LinCMOS op-amps will operate well at low frequencies from a single low-voltage supply. They also require minimum space because of their low component count. The 60 Hz filter illustrated in Figure 3–39 has only one op-amp, three resistors, and three small capacitors.
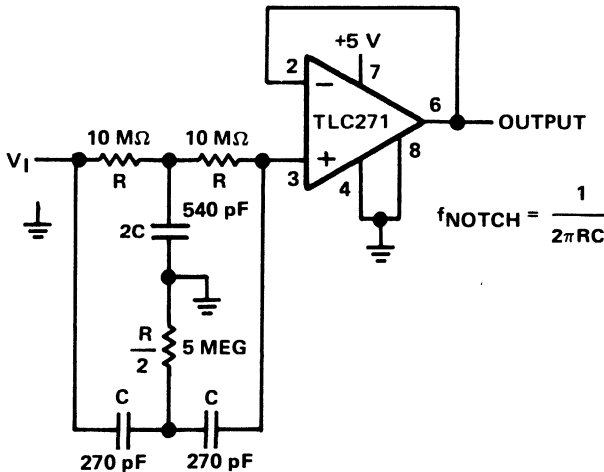
$$f_{NOTCH} = \frac{1}{2\pi RC}$$

Fig. 3–39   Twin-T Notch Filter for 60 Hz.

If the resistors and capacitors are carefully matched, you theoretically obtain almost complete rejection of the 60 Hz null frequency. The TLC271 has an input bias current of about 1 pA and will not generate adverse offset voltages even though the source impedance is 20 MΩ. Low-level 60 Hz ripple will also be attenuated due to the TLC271's capability of handling input signals at the ground rail while operating from a single supply. As illustrated in Figure 3–40, a 39 dB notch was achieved with this circuit.
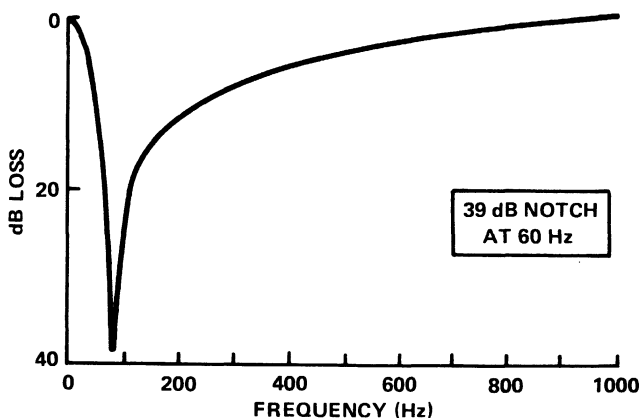
Fig. 3–40   TLC271 Twin-T Notch Filter Frequency Response.

Single Supply Function Generator

A function generator is a circuit that can deliver a number of different waveforms. Some circuits operate at a fixed frequency while others have the capability of varying their frequencies over a wide range. The example circuit shown in Figure 3–41 has both square-wave and triangle-wave output.

The left section is similar in function to a comparator circuit that uses positive feedback for hysteresis. The inverting input is biased at one-half the V_{CC} voltage by resistors R4 and R5. The output is fed back to the noninverting input of the first stage to control the frequency. The amplitude of the square wave is the output swing of the first stage, which is 8 V peak-to-peak.
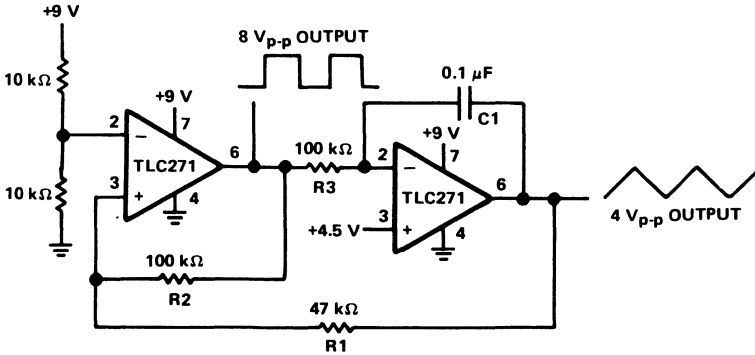
Fig. 3–41   Single Supply Function Generator.

The second stage is basically an op-amp integrator. The resistor R3 is the input element and capacitor C1, is the feedback element. The ratio R1/R2 sets the amplitude of the triangle wave, as referenced to the square-wave output. For both waveforms, the frequency of oscillation can be determined by the equation:

$$fo = \frac{1}{4R3C1}\left[\frac{R2}{R1}\right]$$

The output frequency is approximately 50 Hz with the given components. The different waveforms are illustrated in Figure 3–42.
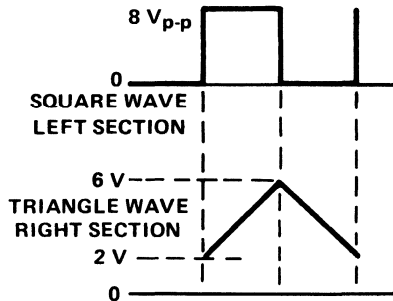
Fig. 3–42   Function Generator Output Waveforms.

COMPARATOR APPLICATIONS

Window Comparator

As the name implies, a window detector is a specialised comparator circuit designed to detect the presence of a voltage between the two prescribed limits that is, within a voltage 'window'. A window comparator is useful in test and production equipment to select components that are within a specific set of limits.

This circuit is implemented by logically combining the outputs of two single-ended comparators. One indicates an input greater than the lower limit, and the other an input less than the upper limit. If both comparators indicate a true condition, the output is true. If either input is not true, the output is not true. A basic window comparator circuit is illustrated in Figure 3–43.
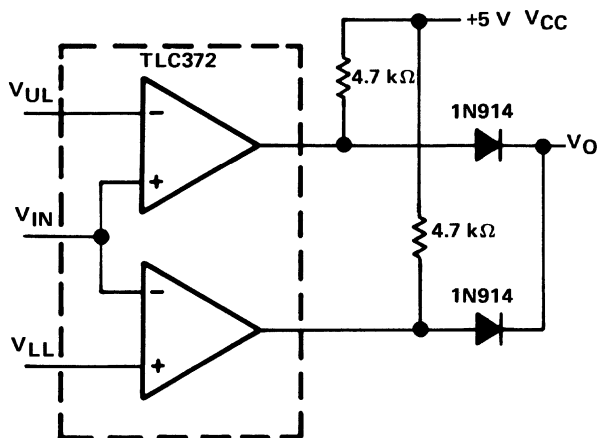
Fig. 3–43   Basic Window Comparator.

In this circuit, the outputs of the two comparators are logically combined by the 1N914 diodes. When the input voltage is between the upper limit (V_{UL}) and the lower limit (V_{LL}) the output voltage is zero; otherwise it equals a logic high level. The output of this circuit can be used to drive a logic gate, LED driver or relay driver circuit. The circuit shown in Figure 3–44 shows a 2N2222 npn transistor being driven by the window comparator. When the input voltage to the window comparator is outside the range set by the V_{UL} and V_{LL} inputs, the output changes to positive, which turns on the transistor and lights the LED indicator.
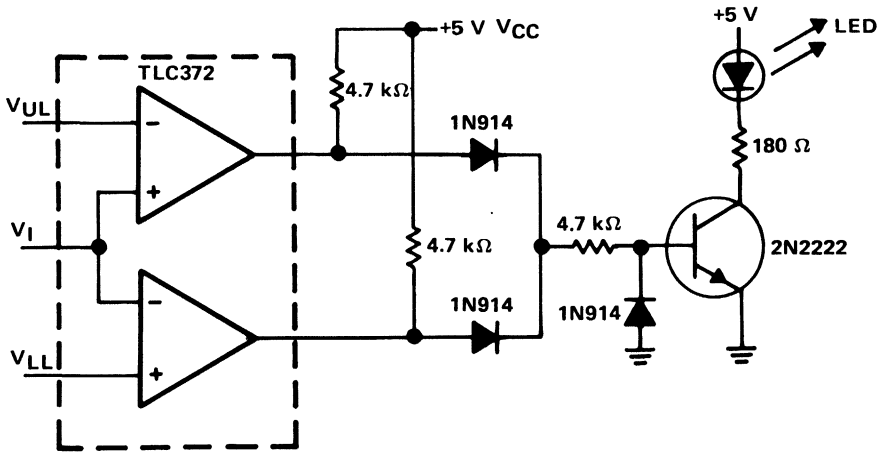
Fig. 3–44   Window Comparator with LED Indicator.

The TLC372 features extremely high input impedance (typically greater than $10^{12}\ \Omega$) which allows direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations, and can be connected to achieve positive-logic wired-AND relationships. While these devices meet the 2000 V ESD (electrostatic discharge) specification, care should be exercised in handling the chips because exposure to ESD may result in a degradation of the device
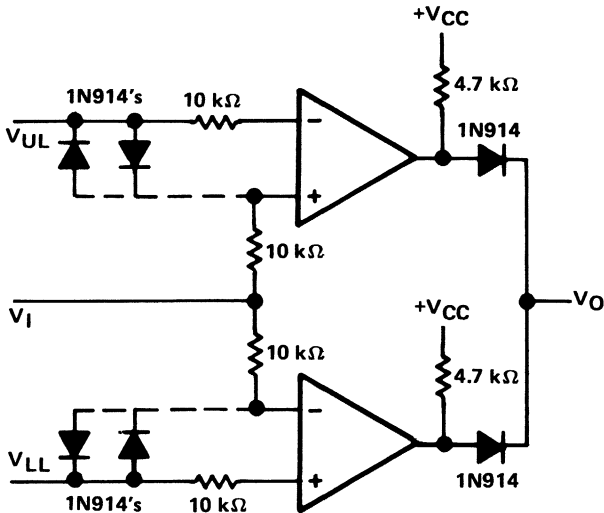
Fig. 3–45   Input Protection Circuitry.

performance. If the input signal will exceed the common-mode voltage, it is good design practice to include protective input circuitry to the comparators. Clamp diodes and/or series resistors, as shown in Figure 3–45, could be used for this purpose.

Comparator Interface Circuits

A comparator is a useful building block in signal conditioning circuits as well as in instrumentation and control circuits. Once the inputs to the comparator have been correctly matched and connected, the comparator must interface with any additional output circuitry to perform functions such as: energizing a relay, lighting a lamp or driving another type of logic circuit.

Figure 3–46 shows three similar output interface circuits which can be used to drive a lamp, a relay, and an LED. All three circuits utilize the popular LM311 comparator and 2N2219/2N3904 family of discrete transistors. A resistor in series with the transistor base should be used in circuits of this type in order to limit the current. Although it is possible to directly drive some small lamps and relays from the output of the comparator, it is advisable to use a buffer transistor as illustrated. The output buffer will minimize loading on the comparator to preserve its gain and drift characteristics, and provide a higher output current.

Figure 3–46(a) is a circuit which can be used to turn on a 28 V lamp. A 100 Ω resistor must be included in series with the lamp. The purpose of this resistor is to limit the cold lamp inrush current. Lower voltage lamps of up to 150 mA current rating can be driven by reducing the lamp supply voltage appropriately.

Figure 3–46(b) illustrates a relay driver circuit. The relay is connected in series with the transistor collector terminal and the 24 V supply. The 1N914 diode across the relay clamps the back EMF voltage generated when the relay is turned off. Lower voltage relays can be driven as well as the relay illustrated here, provided the maximum current is less than 150 mA.

Figure 3–46(c) illustrates an LED driver, using a 2N3904 transistor switch rather than the high-powered 2N2219. The TIL220 is a red LED and has approximately a 1.7 V drop in the forward-bias condition at a
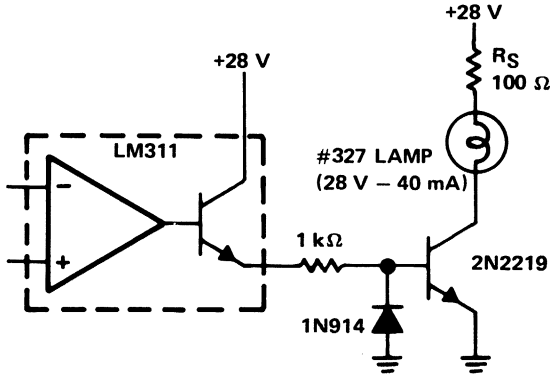
(a) LAMP DRIVER
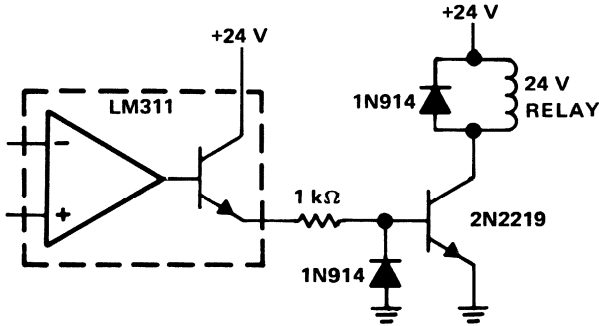
(b) RELAY DRIVER
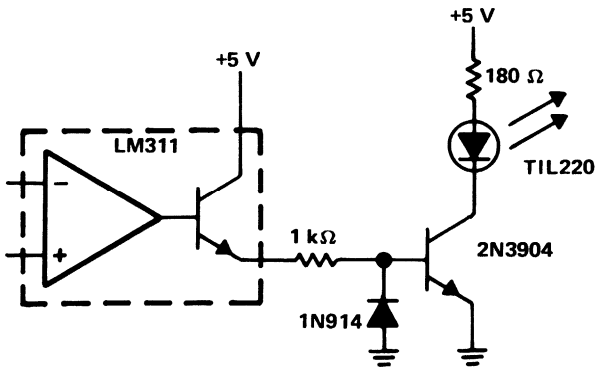
(c) LED DRIVER

Fig. 3–46   Comparator Output Interface Circuits.

forward current of 20 mA with a V_{CC} of 5 V. The value of the current limiting resistor is calculated as shown below:

$$R = \frac{5\,V - 1.7\,V}{0.020\,A} = 165\text{ ohms}$$

The next higher standard value is 180 Ω which has been used in this circuit.

A comparator output may interface with digital logic. If the comparator operates from a single 5 V supply, there is no problem. Interfacing to a comparator that is operating from ±15 V supplies may require some level shifting and/or clamping to drive logic circuits. Figure 3–47 illustrates graphically how to interface comparators to different level logic circuits.

Figure 3–47(a) illustrates a comparator with a single 5 V power supply and has a 10 kΩ pull-up resistor on the output. This circuit will drive standard TTL logic circuits or low-level CMOS logic circuits. These logic circuits require a maximum of 0.8 V for low state and a minimum of 2.4 V for high state.

Figure 3–47(b) illustrates a comparator circuit capable of driving high-level CMOS circuits. This circuit operates from dual 15 V supplies and uses a 100 kΩ pull-up resistor on the output. High-level CMOS logic requires a maximum of 4.0 V for a low state and a minimum of 11.0 V for a high state.

Figure 3–47(c) illustrates how a three-state output is produced by following the comparator with a hex-bus driver such as the SN74367. In this circuit the comparator has a 10 kΩ pull-up resistor on its output and sends TTL logic signals to the input of the hex buffer. The output of the hex buffer is controlled by the input control pin's logic level. When this pin is low the device is enabled and the output is TTL logic. When the input control pin is high there is no output from the device and the output looks like a high impedance.

LM393 Zero-Crossing Detector

A zero-crossing detector is sometimes called a zero-level detector or a Schmitt trigger. In operation, a zero-crossing detector determines if

an input voltage to the comparator is greater or less than zero. In response to this determination, the output voltage of the comparator can assume only two possible states. The output state may be high or low depending upon which comparator input (plus or minus) is used to detect the incoming signal.
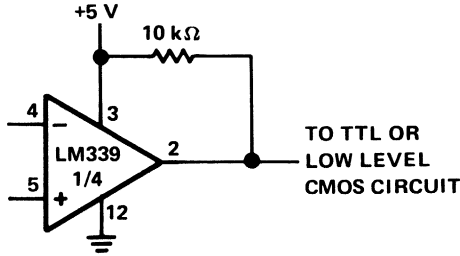
(a) TTL AND LOW-LEVEL CMOS DRIVER
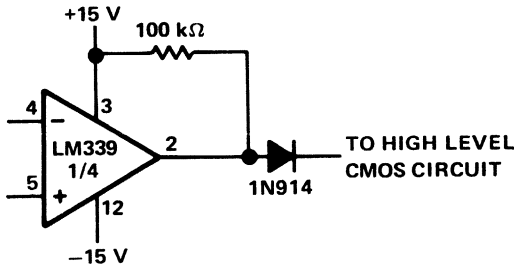
(b) HIGH-LEVEL CMOS DRIVER
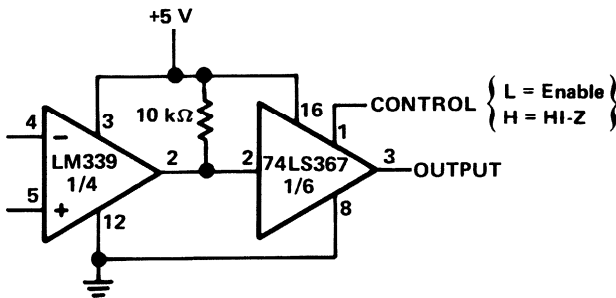
(c) 3-STATE BUS DRIVER (TTL OUTPUT)

Fig. 3–47   Comparator Logic Interface Circuits.

A single comparator may be used as a simple crossover detector, but this can allow several sources of error. These errors may be caused by the input bias and offset currents of the comparator. Temperature may also affect the zero-crossing voltage points. This basic zero-crossing detector also will have another drawback called chatter which is due to noise on the input signal. Chatter can be reduced by adding hysteresis or positive feedback. These provide noise immunity and prevent the output from 'chattering' between states as the input voltage passes through zero.
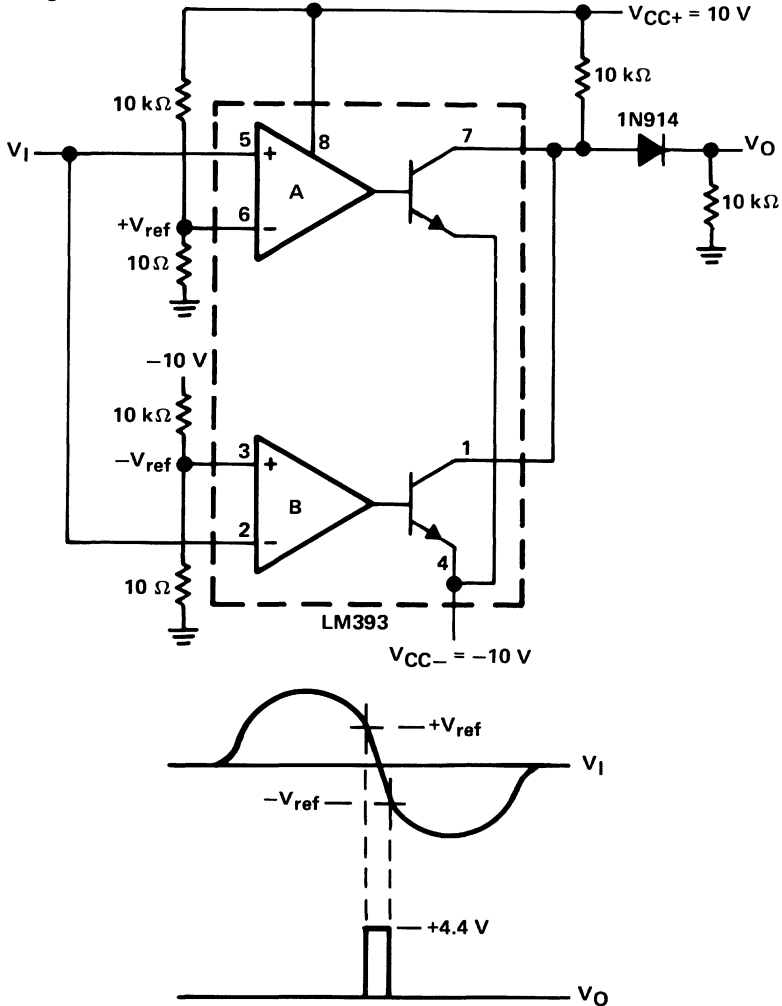
Fig. 3–48   LM393 Zero-Crossing Detector.

An improved circuit is illustrated in Figure 3–48. This zero-crossing detector of this type uses a dual LM393 comparator, and easily controls hysteresis by the reference levels which are set on the comparator inputs.

The circuit illustrated is powered by ±10 V power supplies. The input signal can be an ac signal level up to +8 V. The output will be a positive going pulse of about 4.4 V at the zero-crossover point. These parameters are compatible with TTL logic levels.

The input signal is simultaneously applied to the noninverting input of comparator A and the inverting input of comparator B. The inverting input of comparator A has a +10 mV reference with respect to ground, while the non-inverting input of comparator B has a −10 mV reference with respect to ground. As the input signal swings positive (greater than +10 mV), the output of comparator 'A' will be low while comparator 'B' will have a high output. When the input signal swings negative (less than −10 mV), the reverse is true. The result of the combined outputs will be low in either case. On the other hand, when the input signal is between the threshold points (±10 mV around zero crossover), the output of both comparators will be high. In this state the output voltage will be one-half the 10 V (V_{CC+}) less the 0.6 V diode drop at the junction of the two 10 kΩ resistors (approximately +4.4 V). This circuit is very stable and immune to noise. If more hysteresis is needed, the ± 10 mV window may be made wider by increasing the reference voltages. The 1N914 diode in series with the outputs allows a positive going pulse at the crossover point. This circuit 'squares' the input signal into positive rectangular output pulses whose pulse width corresponds to the input zero crossings.

Section 4

Video Amplifiers

VIDEO AMPLIFIER THEORY

The characteristics of an ideal video amplifier are similar to those of an ideal operational amplifier (i.e. infinite input resistance, infinite gain, zero output resistance, and zero offset).

Typical performance differences between operational amplifiers and video amplifiers are bandwidth and gain. The bandwidth averages 100 kHz for typical operational amplifiers. However, video amplifiers have bandwidths as high as 100 MHz. The gain for a video amplifier averages only 40 dB as compared to 100 dB for operational amplifiers. Because their internal phase shift does not permit the use of negative feedback to control gain, most video amplifiers function only in the open-loop mode. Video amplifiers have a limited output voltage swing. For high-frequency operation, the output voltage swing is limited to a few volts. Table 4–1 lists general characteristics of some video amplifiers which are currently available.

Table 4–1   Video Amplifier Selection Guide.

DEVICE	CHARACTERISTICS	DESCRIPTION
uA733, TL733	– 3 dB bandwidth, 90 MHz	Differential video amplifier. Selectable amplification of 10, 100, or 400.
NE592, SE592	– 3 dB bandwidth, 90 MHz	Differential video amplifier. Selectable amplification of 100 or 400. Adjustable gain from 0 to 400. Adjustable passband.
TL592	– 3 dB bandwidth, 90 MHz	Differential video amplifier. Adjustable gain from 0 to 400. Adjustable passband.
MC1445	– 3 dB bandwidth, 50 MHz	2-channel-input video amplifier. Gate controlled. 16-dB minimum gain. Broadband equivalent input noise, typically 25 μV.

The input stage of most video amplifiers consists of a basic emitter-coupled differential transistor pair connected to a constant-current source transistor. Most early video amplifiers consisted of these three transistors combined with a few integrated resistors and diodes. In addition, all component terminals were brought out for external interconnection. A typical video amplifier configuration is illustrated in Figure 4–1. The bias input voltage can be adjusted to provide

symmetrical output voltage swing with respect to ground.

Video amplifier characteristics are similar to those of operational amplifiers and comparators. However, the following definitions are specifically applicable to video amplifiers.
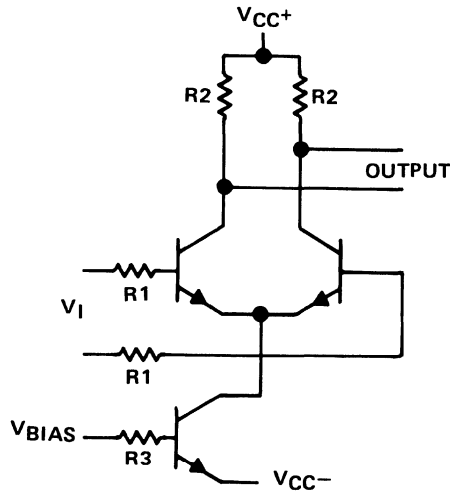
Fig. 4-1   Basic Video Amplifier Circuit.

Voltage Gain

Video amplifiers have a differential type of input and output modes. Voltage gain is defined as the ratio between the change in differential output voltage to the change in differential input voltage as stated in the following equation (see Figure 4-2):

$$A_{VD} = \frac{V_{OD}}{V_{ID}}$$

Common-Mode Output Voltage

With the inputs grounded, the outputs of a video amplifier are at dc

levels with respect to ground. The average of the two dc output voltages is the common-mode output voltage, V_{OC}, and can be determined by the following equation (see Figure 4-2):

$$V_{OC} = \frac{V_O1 + V_O2}{2}$$
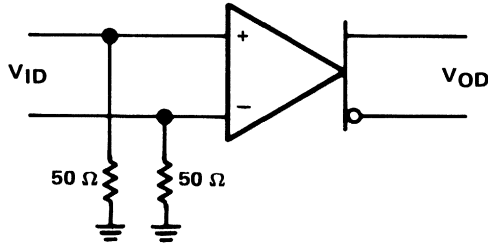
Fig. 4-2   Differential Voltage Gain.

Output Offset Voltage

While functioning under the same conditions as those shown in Figure 4-3, the difference between the dc levels at the two outputs is defined as the output offset voltage ($V_{OO} = V_O1 - V_O2$). The offset voltage can be compared to the input voltage by dividing the offset voltage by the differential voltage gain of the amplifier.
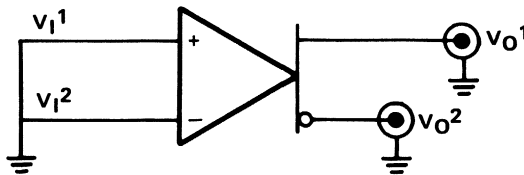
Fig. 4-3   Common-Mode and Offset Voltages.

Video amplifiers have no provision for adjusting the dc input offset voltage. In circuits where this will cause problems, capacitive coupling is used on both the inputs and outputs to block the dc component and prevent it affecting the amplifier signal. Figure 4-4 illustrates the

single-ended and differential coupling methods.
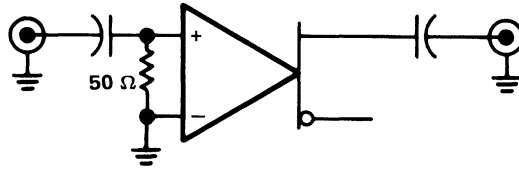
(a) SINGLE-ENDED
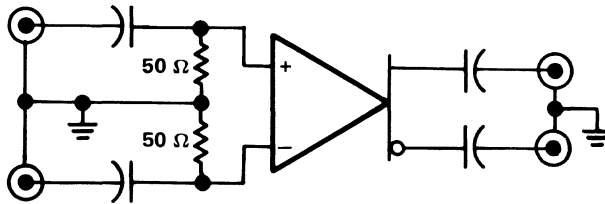
(b) DIFFERENTIAL

Fig. 4–4   Coupling Methods.

Wiring Precautions

The mechanical layout of the video amplifier is very important. All leads should be as short as possible. When using a printed circuit board, conductors should be wide and as short as possible. This helps provide low resistance and low inductance connections. In addition, stray signal coupling from the input to the output is minimized.

Grounding is the most important wiring precaution. As with all high frequency circuits, a ground plane and good grounding techniques should be used. The ground plane should connect all areas of the pattern side of the printed circuit board that are not otherwise used. The ground plane provides a low-resistance low-inductance common return path for all signal and power returns. The ground plane also reduces stray signal pick up.

Each power supply lead should have a bypass capacitor to ground as near as possible to the amplifier pins. A 0.1 μF capacitor is normally sufficient. In the very high-frequency and high-gain circuits, a combina-

tion of a 1 μF tantalum capacitor in parallel with a 470 pF ceramic capacitor is a suitable bypass.

Single point grounding should be used in cases where point-to-point wiring is used or a ground plane is not used. The input signal return, the load signal return, and the power supply common should all be connected at the same physical point. This eliminates ground loops or common current paths which may cause signal modulation or unwanted feedback.

When designing video amplifier circuits, resistor values from 50 Ω to 100 Ω should be used for input terminations. Resistors in this range improve circuit performance by reducing the effects of device input capacitance and input noise currents.

Oscilloscope/Counter Preamplifier
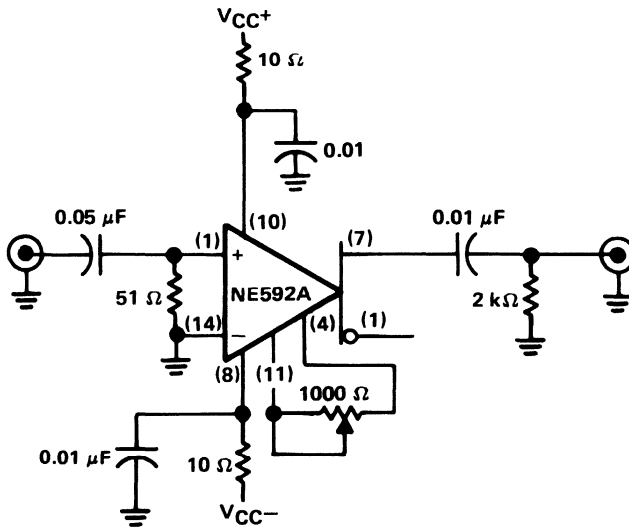
Fig. 4–5   Oscilloscope/Counter Preamplifier Circuit.

A circuit containing a single NE592A video amplifier (the only active component) can be used to increase the sensitivity of an older

oscilloscope or frequency counter. Figure 4–5 shows a circuit which will provide a 20 ±0.1 dB voltage gain from 500 kHz to 50 MHz. The low-frequency response of the amplifier may be extended by increasing the value of the 0.05 μF capacitor connected in series with the input terminal. This circuit will yield an input-noise level of approximately 10 μV over a 15.7 MHz bandwidth.

The gain can be calibrated by adjusting the potentiometer connected between pins 4 and 11 (gain adjust terminals). These pins go directly to the emitter terminals of the two npn differential input amplifiers. The 1000 Ω potentiometer (a cermet type trimmer) can be adjusted for an exact voltage gain of 10. This preserves the scale factor of the instrument. The usual precautions of short leads and wide area ground planes for low-inductance ground systems, should result in good high-frequency response. A compact assembly package for an oscilloscope/counter preamplifier can be made by forming a small piece of sheet copper or brass into the shape of a U.

NE592 Filter Applications
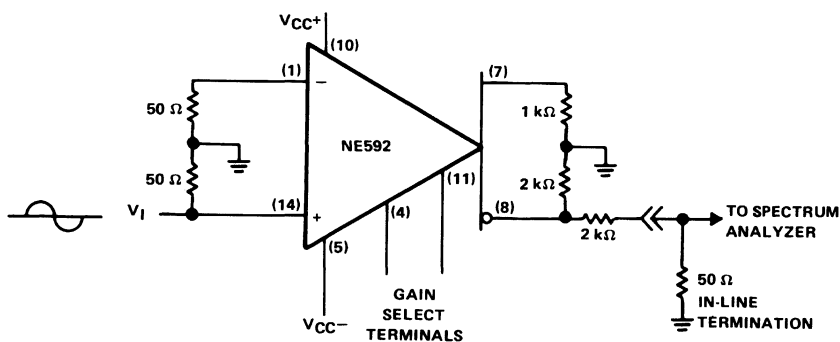
Fig. 4–6   Basic Filter Circuit.

The NE592 is a two-stage differential-output wideband video amplifier. It has a voltage gain of 0 to 400 that can be adjusted by one external resistor. The input stage is designed so that by adding a few external reactive elements between the gain-select terminals (pins 4 and

11), the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems. Figure 4–6 illustrates the basic filter circuit. This circuit has a 50 Ω input termination and a 50 Ω output termination and uses a ±6 V power supply. The 50 Ω output termination allows interfacing to the spectrum analyzer.

Figure 4–7 illustrates the results when five different reactive elements are placed across the gain select terminals (pins 4 and 11). The parametric values and condition of each circuit, as well as the scope photos, are shown.

3.58 MHz

4 ——————||□||—————— 11

GAIN = 40 dB AT PEAK
f_o = 3.6 MHz
3 dB BANDWIDTH 0.5 kHz

(a) CRYSTAL FILTER ELEMENT

10 μH

32 Ω

4 ——/\/\/——————— 11

390 pF

GAIN = 37 dB
NOTCH = 40 dB
f_o = 2.5 MHz
3 dB BANDWIDTH 50 kHz

(b) NOTCH FILTER

32 Ω   390 pF   10 μH

4 ——/\/\/———||————mmm—— 11

GAIN = 37 dB
f_o = 2.6 MHz
3 dB BANDWIDTH 1 MHz

(c) BANDPASS FILTER

Fig. 4–7   Reactive Component Application.

32 Ω   390 pF

4 ——WW——| |—— 11
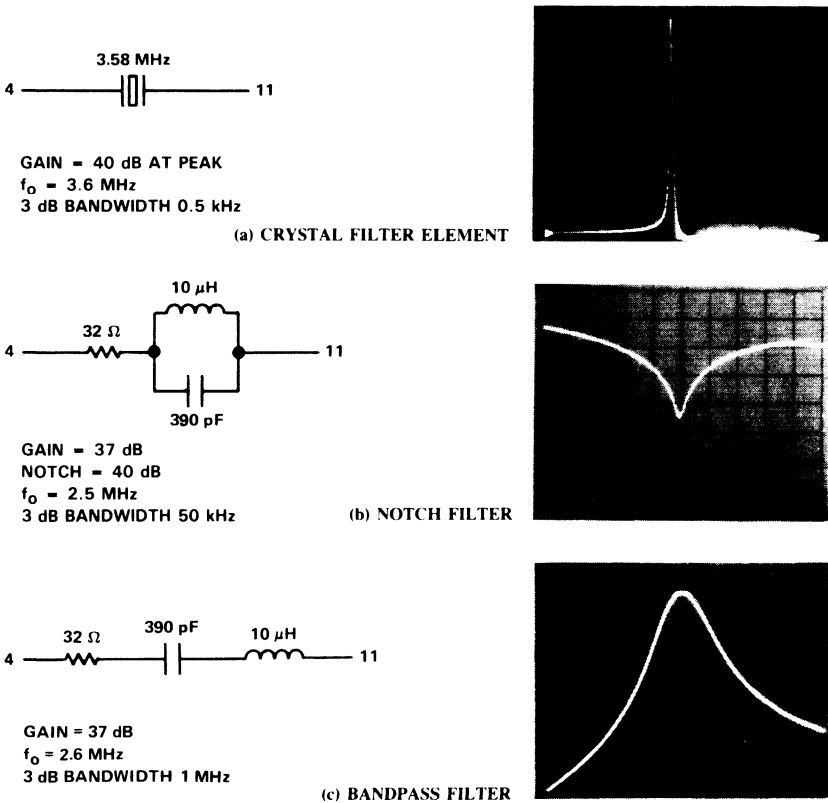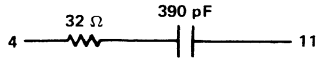
GAIN = 37 dB AT 10 MHz
ROLL-OFF = −40 dB

(d) HIGH-PASS FILTER

32 Ω   10 μH

4 ——WW——⌒⌒⌒—— 11
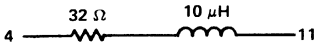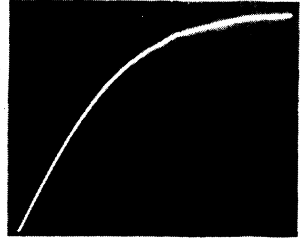
GAIN = 37 dB
28 dB DOWN AT 20 MHz
48 dB DOWN AT 30 MHz

(e) LOW-PASS FILTER
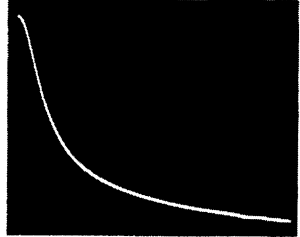
Fig. 4-7   Reactive Component Application (Cont.)

MC1445 Balanced Modulator
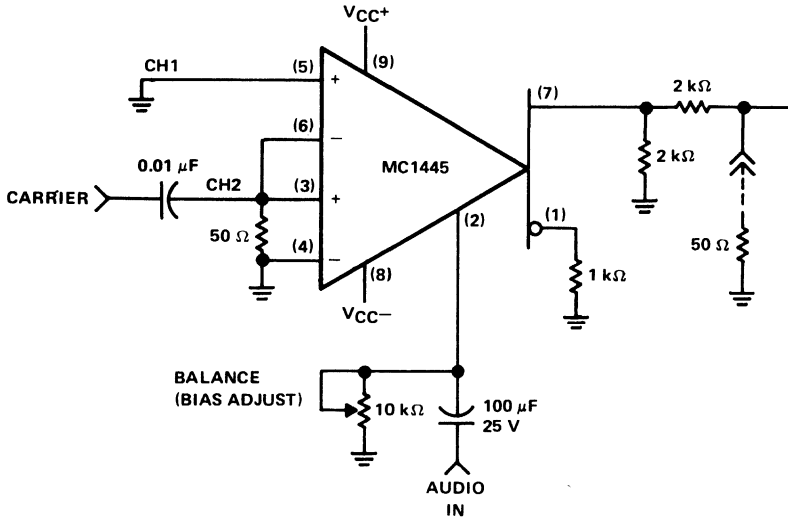
Fig. 4-8   Balanced Modulator.

A balanced modulator can be obtained by connecting an MC1445 gate controlled 2 channel-input video amplifier as shown in Figure 4–8. The internal differential amplifiers are connected in a manner which cross couples the collectors (see Figure 4–9).
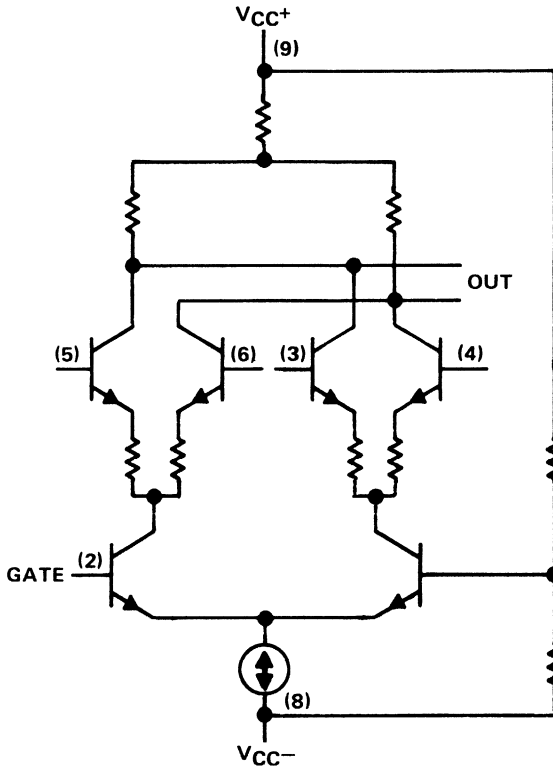
Figure 4–9   Circuit Showing Cross-Coupling.

When the carrier level is adequate to switch the cross-coupled pair of differential amplifiers, the modulation signal (which has been applied to the gate) will be switched, at the carrier rate, between the collector loads. When switching occurs, it will result in the modulation being multiplied by a symmetrical switching function. If the modulation gate remains in the linear region, only the first harmonic of the modulation will be present. To achieve good harmonic suppression of the

modulation input, its input level must remain in the linear region of the gate.

To balance the MC1445 modulator, equal gain must be achieved in the two separate channels. In Figure 4–10 (the composite gate characteristic for both channels) the equal gain point is at 1.3 V. The midpoint of the linear region of channel B is at 1.2 V. To remain in the linear region, the modulation input must be restricted to approximately 200 mV peak-to-peak. Because the carrier suppression is sensitive to the gate bias point a high-resolution (10-turn) potentiometer should be used.
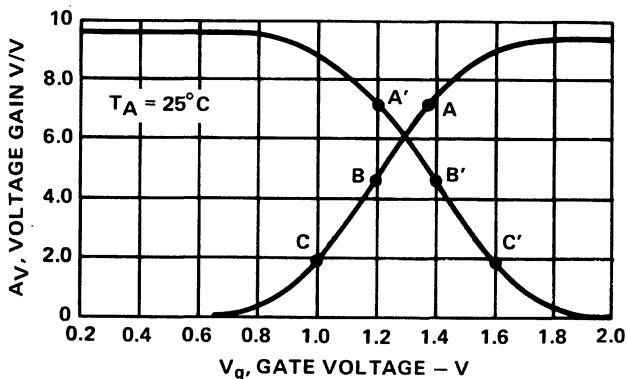
Fig. 4–10   Voltage Gain vs Gate Voltage.

In Figure 4–11, the top trace shows the 1 MHz carrier being modulated by a 1 kHz signal. The output is 750 mV peak-to-peak. The bottom trace shows the 600 mV peak-to-peak 1 kHz modulating signal. When functioning under these conditions, a carrier rejection of 38 dB should be obtained.
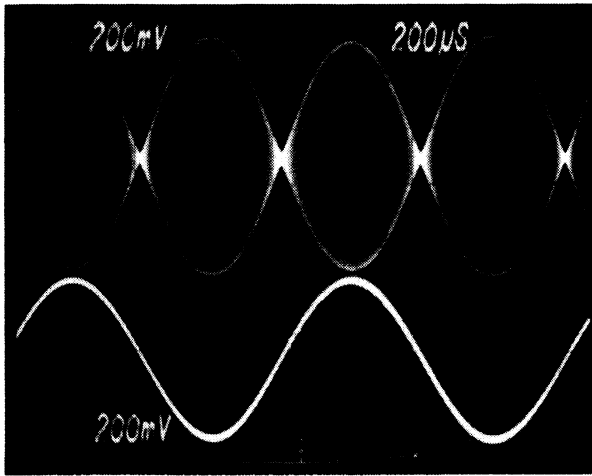
Fig. 4–11   Balanced Modulation.

MC1445 Frequency Shift Keyer

To construct a frequency shift keyer with an MC1445, apply a signal to each differential amplifier input pair. When the gate voltage is changed from one extreme to the other, the output may be switched alternately between the two input signals (see Figure 4–12).
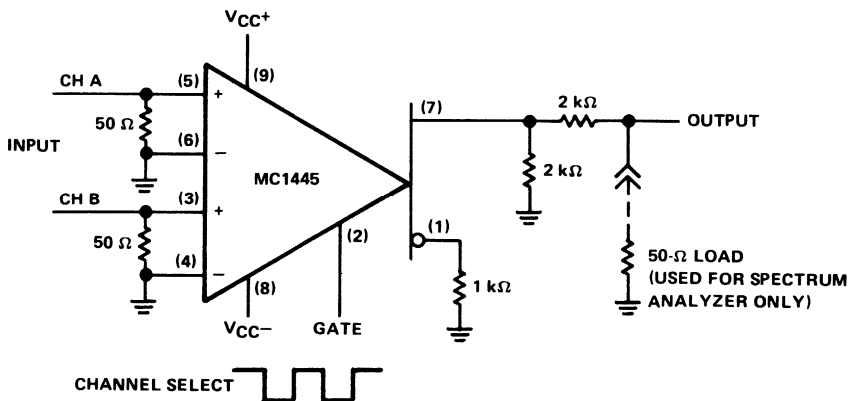
Fig. 4–12   Frequency Shift Keying Test Circuit.

When the gate level is high (1.5 V), a signal applied between pins 5 and 6 (channel A) will be passed and a signal applied between pins 3 and 4 (channel B) will be suppressed. The reverse situation will exist when the gate is low (0.5 V). At 0.5 V, a signal applied to pins 3 and 4 (channel B) will pass. The unselected channel will have a gain of one or less. In this manner, a binary-to-frequency conversion is obtained that is directly related to the binary sequence which is driving the gate input (pin 2). Figure 4–13 illustrates the waveforms of this basic frequency shift keying (FSK) application using the MC1445. The top trace illustrates a 20 kHz signal applied to channel A and a 4 kHz signal applied to channel B. The bottom trace illustrates a 1 kHz gating signal applied to the gate pin (2). The oscilloscope is triggered by this gate input signal.
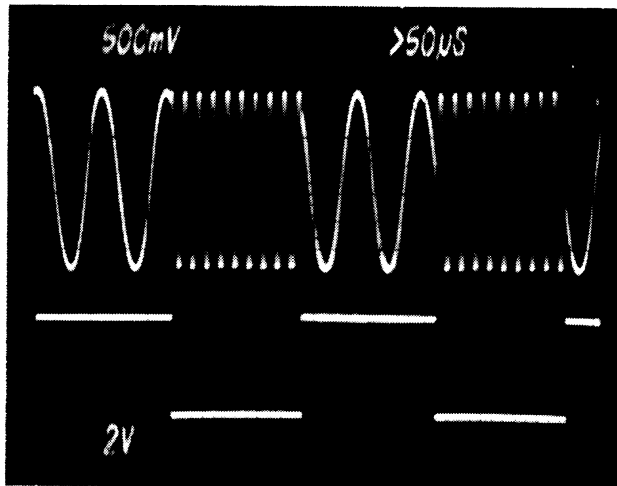
Fig. 4–13   FSK Output and Gate Input Signal Waveforms.

Section 5

Voltage Regulators

BASIC REGULATOR THEORY

The function of every voltage regulator is to convert a dc input voltage into a specific, stable, dc output voltage and maintain that voltage over a wide range of load current and input voltage conditions. To accomplish this, the typical voltage regulator (Figure 5–1) consists of:

1. A reference element that provides a known stable voltage level, (V_{REF}).

2. A sampling element to sample the output voltage level.

3. An error-amplifier element for comparing the output voltage sample to the reference and creating an error signal.

4. A power control element to provide conversion of the input voltage to the desired output level over varying load conditions as indicated by the error signal.
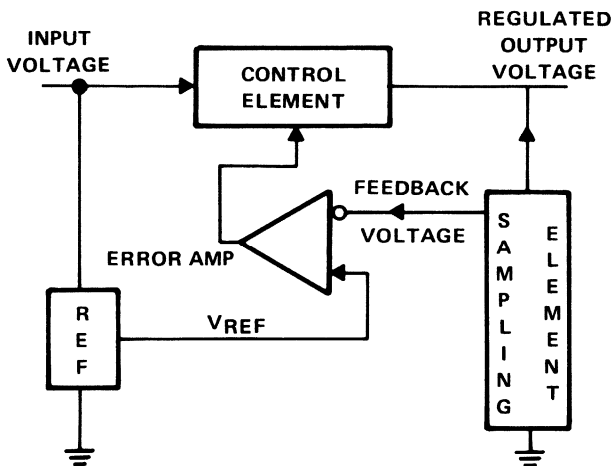
Fig. 5–1   Basic Regulator Block Diagram.

Although actual circuits may vary, the three basic regulator types are series, shunt, and switching. The four basic functions listed above exist in all three regulator types.

VOLTAGE REGULATOR COMPONENTS

Reference Elements

The reference element forms the foundation of all voltage regulators since output voltage is directly controlled by the reference voltage. Variations in the reference voltage will be interpreted as output voltage errors by the error amplifier and cause the output voltage to change accordingly. To achieve the desired regulation, the reference must be stable for all variations in supply voltages and junction temperatures. There are several common techniques which can be used to solve design problems using integrated circuit regulators. Many of these techniques are discussed in the section of the text that outlines error contributions.

Sampling Element

The sampling element monitors the output voltage and converts it into a level that is equal to the reference voltage when the output voltage is correct. A variation in the output voltage causes the feedback voltage to change to a value which is either greater or less than the reference voltage. This voltage difference is the error voltage which directs the regulator to make the appropriate response and thus correct the output voltage change.

Error Amplifier

The error amplifier of a voltage regulator monitors the feedback voltage for comparison with the reference. It also provides gain for the detected error level. The output of the error amplifier drives the control circuit to return the output to the preset level.

Control Element

All the previous elements discussed remain virtually unaltered regardless of the type of regulator circuit. The control element, on the other hand, varies widely, depending upon the type of regulator being designed. It is the element that determines the classification of the voltage regulator; series, shunt, or switching. Figure 5–2 illustrates the three basic control element configurations, each of which is discussed in detail. Any control element error is compensated by the feedback from the sampling element which monitors the output voltage. The control element directly affects parameters such as minimum input-to-output voltage differential, circuit efficiency, and power dissipation.

$$V_O = V_I - (R_S)\, I_L$$

(a) SERIES

$$V_O = V_I - R\,(I_L + I_S)$$

(b) SHUNT

$$V_O = V_I\ \frac{t_{on}}{t_{on} + t_{off}}$$

(c) SWITCHING
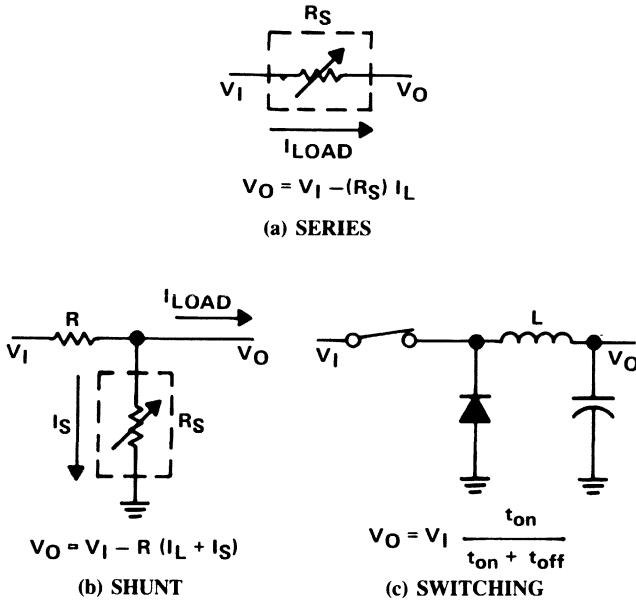
Fig. 5–2   Control Element Configurations.

REGULATOR CLASSIFICATIONS

Series Regulator

The series regulator derives its name from its control element. The output voltage, V_O, is regulated by modulating an active series element,

usually a transistor, that functions as a variable resistor. Changes in the input voltage, V_I, will result in a change in the equivalent resistance of the series element identified as R_S. The product of the resistance, R_S, and the load current, I_L creates a changing input-to-output differential voltage, $V_I - V_O$, that compensates for the changing input voltage. The basic series regulator is illustrated in Figure 5–3, and the equations describing its performance are listed below.

$$V_O = V_{REF} \left(1 + \frac{R1}{R2}\right)$$
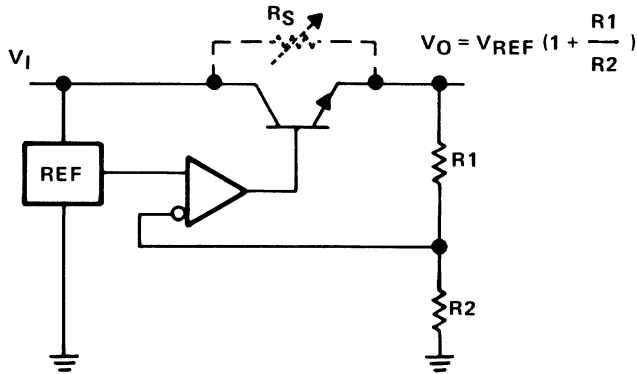
Fig. 5–3   Basic Series Regulator.

$$V_O = V_I - I_L R_S$$

The change in R_S for a changing input voltage is:

$$\Delta R_S = \frac{\Delta V_I}{I_L}$$

The change in R_S for a changing load current:

$$\Delta R_S = \frac{\Delta I_L R_S}{I_L + \Delta I_L}$$

Series regulators provide a simple, inexpensive way to obtain a source of regulated voltage. In high-current applications, however, the voltage drop which is maintained across the control element will result in substantial power loss and a much lower efficiency regulator.

Shunt Regulator

The shunt regulator employs a shunt control element in which the current is controlled to compensate for varying input voltage or changing load conditions. The basic shunt regulator is illustrated in Figure 5-4.
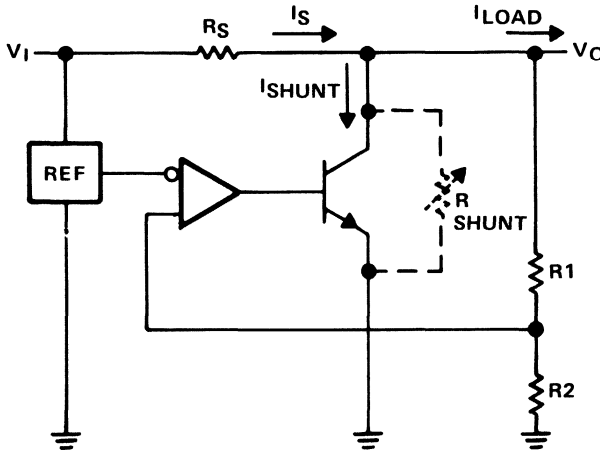
Fig. 5-4   Basic Shunt Regulator.

As I_{LOAD} increases, $I_{(shunt)}$ decreases to adjust the voltage drop across R_S. In this fashion V_O is held constant.

$$V_O = V_I - I_S R_S$$

$$I_S = I_L + I_{(shunt)}$$

$$V_O = V_I - R_S[I_L + I_{(shunt)}]$$

The change in shunt current for a changing load current is:

$$\Delta I_{(shunt)} = -\Delta I_L$$

The change in shunt current for a changing input voltage is:

$$\Delta I_{(shunt)} = \frac{\Delta V_I}{R_S}$$

$$I_{(shunt)} = \frac{V_O}{R_{(shunt)}}$$

Even though it is usually less efficient than series or switching regulators, a shunt regulator may be the best choice for some applications. The shunt regulator is less sensitive to input voltage transients; does not reflect load current transients back to the source, and is inherently short-circuit proof.

Switching Regulator

The switching regulator employs an active switch as its control element. This switch is used to chop the input voltage at a varying duty cycle based on the load requirements. A basic switching regulator is illustrated in Figure 5–5.
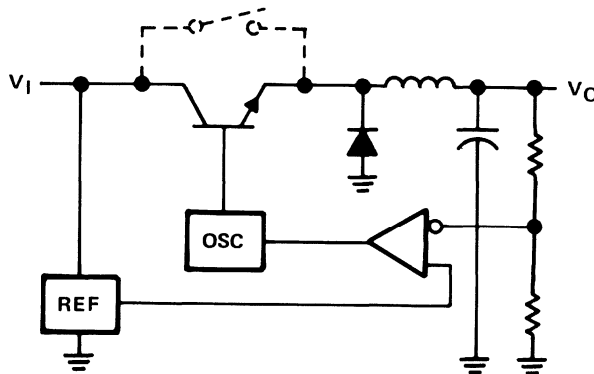
Fig. 5–5   Basic Switching Regulator (Step-Down Configuration).

A filter, usually an LC filter, is then used to average the voltage present at its input and deliver that voltage to the output load. Because the pass transistor is either on (saturated) or off, the power dissipated in the control element is minimal. The switching regulator is therefore more efficient than the series or shunt type. For this reason, the switching regulator becomes particularly advantageous for applications involving large input-to-output differential voltages or high load-current requirements. In the past, switching voltage regulators were discrete designs. However, recent advancements in integrated circuit technology have resulted in several monolithic switching regulator circuits that contain all of the necessary elements to design step-up, step-down, or inverting voltage converters.

Duty cycle variation is usually achieved by maintaining a constant frequency and varying the on-off times. This is known as pulse width modulation (PWM). An alternative technique is to maintain a constant on-time and vary the off-time (varying the frequency).

MAJOR ERROR CONTRIBUTIONS

The ideal voltage regulator maintains constant output voltage despite varying input voltage, load current, and temperature conditions. Realistically, these influences affect the regulator's output voltage. In addition, the regulator's own internal inaccuracies affect the overall circuit performance. This section discusses the major error contributors, their effects, and suggests some possible solutions to the problems they create.

Regulator Reference Techniques

There are several reference techniques employed in integrated circuit voltage regulators. Each provides its particular level of performance and problems. The optimum reference depends on the regulator's requirements.

Zener Diode Reference

The zener diode reference, as illustrated in Figure 5-6, is the simplest technique. The zener voltage itself, V_Z, forms the reference voltage, V_{REF}.
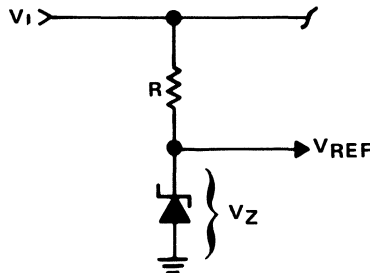
Fig. 5-6   Basic Zener Reference.

This technique is satisfactory for relatively stable supply-voltage and load-current applications. The changing zener current results in an error in the zener diode's reference voltage, V_Z, due to the zener impedance. This zener reference model is illustrated in Figure 5–7.

$$V_{REF} = V_Z = V_{Z'} + R_Z \left(\frac{V_I - V_{Z'}}{R + R_Z} \right)$$
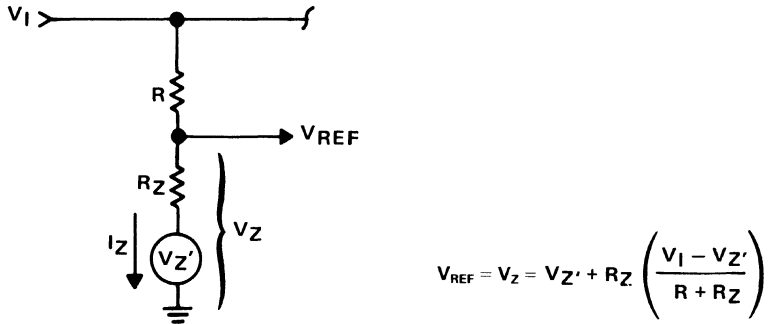
Fig. 5–7   Zener Reference Model.

Constant-Current Zener Reference

The zener reference can be refined by the addition of a constant-current source as its supply. Driving the zener diode with a constant current minimizes the effect of zener impedance in the overall stability of the zener reference. An example of this technique is illustrated in Figure 5–8. The reference voltage of this configuration is relatively independent of changes in supply voltage and load current.
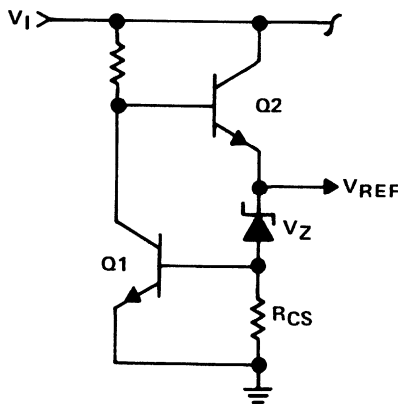
Fig. 5–8   Constant-Current Zener Reference.

$$V_{REF} = V_Z + V_{BE(Q1)}$$

$$I_Z = \frac{V_{BE(Q1)}}{R_{CS}}$$

In addition to superior supply voltage independence, the circuit illustrated in Figure 5–8 yields improved temperature stability. The reference voltage, V_{REF}, is the sum of the zener voltage (V_Z) and the base-emitter voltage of Q1[$V_{BE(Q1)}$]. A low temperature coefficient can be achieved by balancing the positive temperature coefficient of the zener with the negative temperature coefficient of the base-emitter junction of Q1.

Band-Gap Reference

Another popular reference is the band-gap reference, which developed from the highly predictable emitter-base voltage of integrated transistors. Basically, the reference voltage is derived from the energy-band-gap voltage of the semiconductor material [$V_{go(silicon)}$ = 1.204 V]. The basic band-gap configuration is illustrated in Figure 5–9. The reference voltage, V_{REF}, in this case is:

$$V_{REF} = V_{BE(Q3)} + I_2 R_2$$
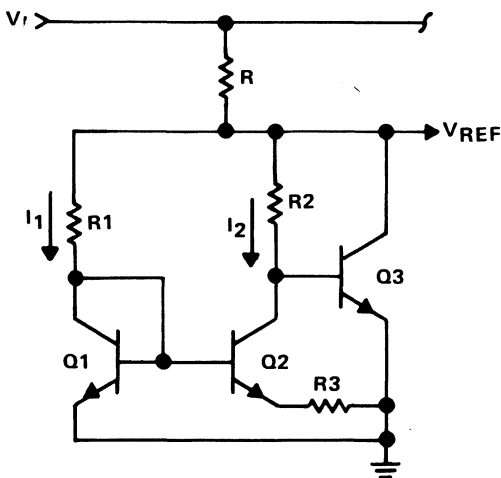
Fig. 5–9   Band-Gap Reference.

The resistor values of R1 and R2 are selected in such a way that the current through transistors Q1 and Q2 are significantly different ($I_1 = 10I_2$). The difference in current through transistors Q1 and Q2 also results in a difference in their respective base-emitter voltages. This voltage differential $[V_{BE(Q1)} - V_{BE(Q2)}]$ will appear across R3. Application of transistors with sufficiently high gain results in current I_2 passing through R3. In this instance, I_2 is equal to:

$$\frac{V_{BE(Q1)} - V_{BE(Q2)}}{R3}$$

$$\therefore V_{REF} = V_{BE(Q3)} + \left[\left(V_{BE(Q1)} - V_{BE(Q2)}\right)\frac{R2}{R3}\right]$$

By analyzing the effect of temperature on V_{REF} it can be shown that the difference between two similar transistors' emitter-base voltages, when operated at different currents is:

$$V_{BE(Q1)} - V_{BE(Q2)} = \frac{kT}{q}\ln\frac{I_1}{I_2}$$

where

  k = Boltzmann's constant

  T = absolute temperature − degrees K

  q = charge of an electron

  I = current

The base-emitter voltage of Q3 can also be expressed as:

$$V_{BE(Q3)} = V_{go}\left[1 - \frac{T}{T_O}\right] + V_{BEO}\left[\frac{T}{T_O}\right]$$

where

  V_{go} = band-gap potential

  V_{BEO} = emitter-base voltage at T_O

V_{REF} can then be expressed as:

$$V_{REF} = V_{go}\left[1 - \frac{T}{T_O}\right] + V_{BEO}\left[\frac{T}{T_O}\right]$$
$$+ \frac{R2}{R3} \quad \frac{kT}{q} \ln\frac{I_1}{I_2}$$

Differentiating with respect to temperature yields

$$\frac{dV_{REF}}{dT} = -\frac{V_{go}}{T_O} + \frac{V_{BEO}}{T_O} + \frac{R2}{R3} \quad \frac{k}{q} \ln\frac{I_1}{I_2}$$

If R2, R3, and I_1 are appropriately selected such that

$$\frac{R2}{R3} \ln\frac{I_1}{I_2} = [V_{go} - V_{BEO(Q3)}] \, C$$

where

$$C = \frac{q}{kT_O}$$

and

$$V_{go} = 1.2 \text{ V}$$

the resulting

$$\frac{dV_{REF}}{dT} = 0$$

The reference is temperature-compensated.

Band-gap reference voltage is particularly advantageous for low-voltage applications ($V_{REF} = 1.2$ V) and it yields a reference level that is stable even with variations in supply and temperature.

Sampling Element

The sampling element used on most integrated circuit voltage regulators is an R1/R2 resistor divider network (Figure 5–10), which can be determined by the output-voltage-to-reference-voltage ratio.

$$\frac{V_O}{V_{REF}} = 1 + \frac{R1}{R2}$$
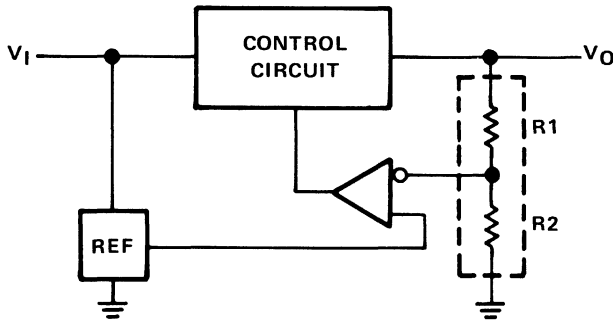
Fig. 5–10   R1/R2 Ladder Network Sampling Element.

Since the feedback voltage is determined by ratio and not absolute value, proportional variations in R1 and R2 have no effect on the accuracy of the integrated circuit voltage regulator. When proper attention is given to the layout of these resistors in an integrated circuit, their contribution to the error of the voltage regulator will be minimal. The initial accuracy is the only parameter affected.

Error Amplifier Performance

If a stable reference and an accurate output sampling element exist, the error amplifier becomes the primary factor determining the performance of the voltage regulator. Typical amplifier performance parameters such as offset, common-mode and supply-rejection ratios, output impedance, and temperature coefficient affect the accuracy and regulation of the voltage regulator. These amplifier performance parameters will affect the accuracy of the regulator due to variations in supply, load, and ambient temperature conditions.

Offset Voltage

Offset voltage is viewed by the amplifier as an error signal, as illustrated in Figure 5–11, and will cause the output to respond accordingly.
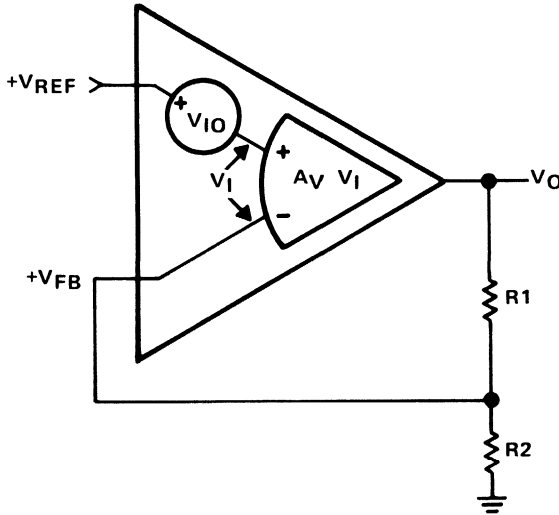
Fig. 5–11   Amplifier Model Showing Input Offset Voltage Effect.

$$V_O = A_V V_I$$

$$V_I = V_{REF} - V_{IO} - V_{FB}$$

$$V_{FB} = V_O \frac{R2}{R1 + R2}$$

$$V_O = \frac{V_{REF} - V_{IO}}{\dfrac{1}{A_V} + \left[\dfrac{R2}{R1 + R2} \right]}$$

If A_V is sufficiently large

$$V_O = (V_{REF} - V_{IO}) \left[1 + \frac{R1}{R2} \right]$$

V_{IO} represents an initial error in the output of the integrated circuit voltage regulator. The simplest method of compensating for this error is to adjust the output voltage sampling element R1/R2.

Offset Change with Temperature

The technique discussed above compensates for the amplifier's offset voltage and yields an accurate regulator, but only at a specific temperature. In most amplifiers, the offset voltage change with temperature is proportional to the initial offset level. Trimming the output voltage sampling element, does not reduce the offset voltage but merely counteracts it. At a different ambient temperature, the offset voltage changes and, thus, error is again introduced into the voltage regulator. Monolithic integrated circuit regulators use technology that essentially eliminates offset in integrated circuit amplifiers. With minimal offset voltage, drift caused by temperature variations will have little consequence.

Supply Voltage Variations

The amplifier's power supply and common-mode rejection ratios are the primary contributors to regulator error which has been introduced by an unregulated input voltage. In an ideal amplifier, the output voltage is a function of the differential input voltage only. Realistically, the common-mode voltage of the input also influences the output voltage. The common-mode voltage is the average input voltage, referenced from the amplifier's virtual ground (see Figure 5–12 and the following equations).
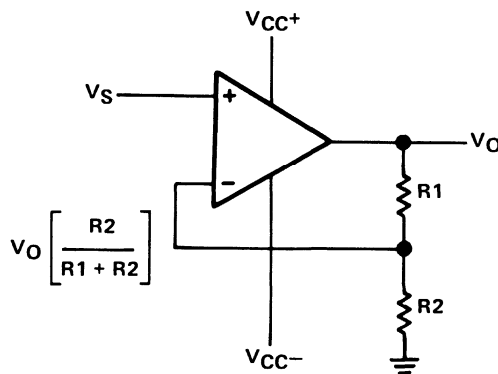
Fig. 5–12   Amplifier Model Showing Common-Mode Voltage.

$$\text{Virtual Ground} = \frac{V_{CC+} + V_{CC-}}{2}$$

$$V_{I(av)} = \frac{V_S + V_O\left[\dfrac{R2}{R1 + R2}\right]}{2}$$

$$V_{CM} = \frac{1}{2}\left[V_S + V_O\left(\frac{R2}{R1 + R2}\right) - \left(V_{CC+} + V_{CC-}\right)\right]$$

From this relation it can be seen that unequal variations in either power supply bus rail will result in a change in the common-mode voltage.

The common-mode voltage rejection ration (CMRR) is the ratio of the amplifier's differential voltage amplification to the common-mode voltage amplification.

$$CMRR = \frac{A_{VD}}{A_{VCM}}$$

$$A_{VCM} = \frac{A_{VD}}{CMRR}$$

That portion of output which is voltage contributed by the equivalent common-mode input voltage is:

$$V_O = V_{CM}A_{VCM} = \frac{A_{VD}V_{CM}}{CMRR}$$

The equivalent error introduced then is:

$$\text{COMMON-MODE ERROR} = \frac{V_{CM}}{CMRR}$$

The common-mode error represents an offset voltage to the amplifier. Neglecting the actual offset voltage, the output voltage of the error amplifier then becomes:

$$V_O = \left(V_{REF} + \frac{V_{CM}}{CMRR}\right)\left(1 + \frac{R1}{R2}\right)$$

Using constant-current sources in most integrated circuit ampli-
fiers, however, yields a high power-supply (common-mode) rejection
ratio. This power-supply rejection ratio is of such a large magnitude that
the common-mode voltage effect on V_O can usually be neglected.

REGULATOR APPLICATION CONSIDERATIONS

Various types of integrated circuit voltage regulators are available,
each having its own particular characteristics, giving it advantages in
various applications. The type of regulator used depends primarily upon
the designer's needs and trade-offs in performance and cost.

Positive Versus Negative Regulators

Most applications use regulators in the conventional manner;
positive and negative regulators regulate respective positive and
negative voltages. However, it is possible to use them interchangeably
in ground isolated configurations.

Figure 5–13 illustrates conventional positive and negative voltage
regulator applications employing a continuous and common ground.
For systems operating with a single supply, the positive and negative
regulators may be interchanged by floating the ground reference to the
load or input. This approach to design is recommended only where
ground isolation serves as an advantage to overall system performance.
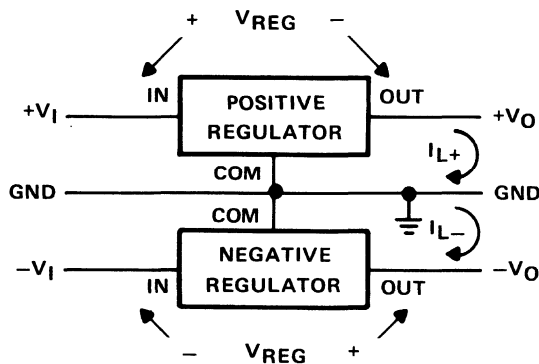
Fig. 5–13   Conventional Positve/Negative Regulator.

Figure 5–14 and 5–15 illustrate a positive regulator in a negative configuration and a negative regulator in a positive configuration, respectively.
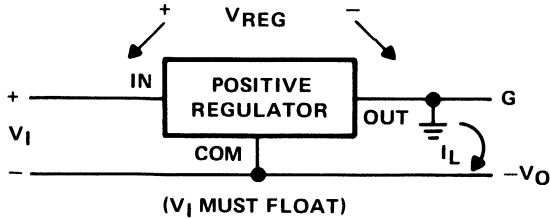
*Fig. 5–14   Positive Regulator in Negative Configuration
(V_I Must Float).*
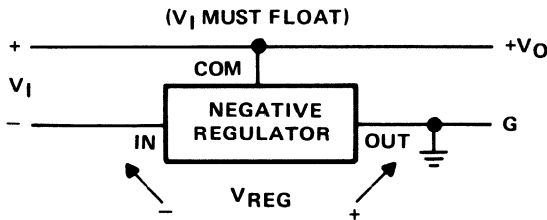
*Fig. 5–15   Negative Regulator in Positive Configuration
(V_I Must Float).*

Fixed Versus Adjustable Regulators

Many fixed three-terminal voltage regulators are available in various current ranges from most major integrated circuit manufacturers. These regulators offer the designer a simple, inexpensive method to establish a regulated voltage source. Their particular advantages are:

1. Ease of use

2. Few external components required

3. Reliable performance

4. Internal thermal protection

5. Short-circuit protection

There are disadvantages. The fixed three-terminal voltage regulators cannot be precisely adjusted because their output voltage sampling elements are internal. The initial accuracy of these devices may vary as much as ±5% from the nominal value; also the output voltages available are limited.

Current limits are based on the voltage regulator's applicable current range and are not adjustable. Listings of some fixed and variable voltage regulators are given at the end of this chapter. Extended range operation (increasing I_{LOAD}) is cumbersome and requires complex external circuitry.

The adjustable regulator may be well suited for those applications requiring higher initial accuracy. This depends on the complexity of the adjustable voltage regulator. Additionally, all adjustable regulators use external feedback, which allows the designer a precise and infinite voltage selection.

The output sense may also be referred to a remote point. This allows the designer to not only extend the range of the regulator (with minimal external circuitry), but also to compensate for losses in a distributed load or external pass components. Additional features found on many adjustable voltage regulators are: adjustable short-circuit current limiting, access to the voltage reference element, and shutdown circuitry.

Dual-Tracking Regulators

The dual tracking regulator (Figure 5–16) provides regulation for two power supply buses, usually one positive and one negative. The dual-tracking feature assures a balanced supply system by monitoring the voltage on both power supply buses. If either of the voltages sags or goes out of regulation, the tracking regulator will cause the other voltage to vary accordingly. (A 10% sag in the positive voltage will result in a 10% sag in the negative voltage.) These regulators are, for the most part, restricted to applications such as linear systems where balanced supplies offer a definite performance improvement.
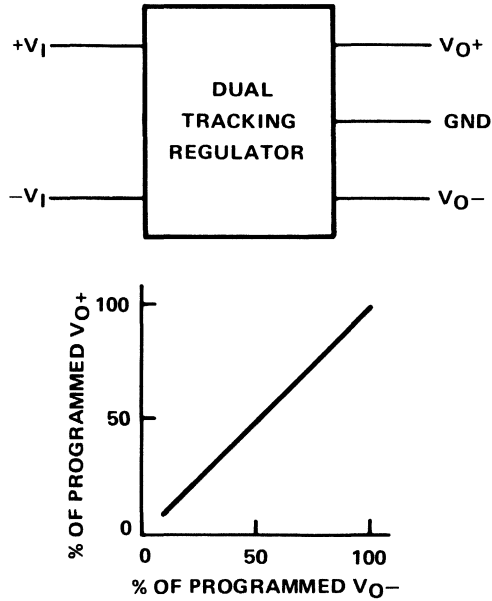
Fig. 5–16   Dual Tracking Regulator.

Series Regulators

The series regulator is well suited for medium current applications with nominal voltage differential requirements. Modulation of a series pass control element to maintain a well regulated, prescribed, output voltage is a straightforward design technique. Safe-operating-area protection circuits such as overvoltage, fold-back current limiting, and short-circuit protection are additional functions that series regulators can supply. The primary disadvantage of the series regulator is its power consumption. The amount of power a series regulator (Figure 5–17) will
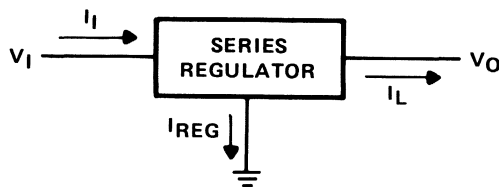
Fig. 5–17   Series Regulator.

consume depends on the load current being drawn from the regulator and is proportional to the input-to-output voltage differential. The amount of power consumed becomes considerable with increasing load or differential voltage requirements. This power loss limits the amount of power that can be delivered to the load because the amount of power that can be dissipated by the series regulator is limited.

The equations that describe these conditions are listed below. P_{REG} is the power lost in the regulator, I_I is the input current, I_{REG} is the regulator current and I_L is the load current. The differential voltage across the regulator is $(V_I - V_O)$.

$$P_{REG} = V_I I_I - V_O I_L$$

$$I_I \quad = I_{REG} + I_L$$

Since I_L is much greater than I_{REG}

$$I_I \quad = I_L$$

$$P_{REG} = I_L (V_I - V_O)$$

Adjustable (Floating) Regulator

The adjustable regulator (Figure 5–18) is a series regulator with external output adjustment. The output voltage is set by a potential
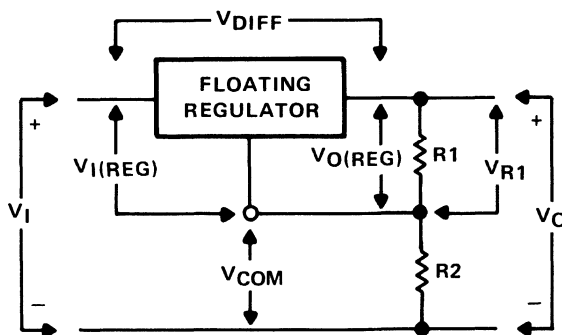
Fig. 5–18   Adjustable Regulator

divider (R1/R2). Regulation is achieved by the control element adjusting the input/output differential until the voltage across R1, ($V_{O(REG)}$) is equal to the internal reference.

$$V_{O(reg)} = V_{REF} = V_{R1}$$

$$V_{R1} = V_O \left[\frac{R1}{R1 + R2} \right]$$

$$V_O = V_{REF} \left[1 + \frac{R2}{R1} \right]$$

The regulator is 'floating' above the ground with a common terminal voltage of:

$$V_{COM} = V_O - V_{R1} = V_O - V_{REF}$$

The input voltage seen by the adjustable regulator is:

$$V_{I(reg)} = V_I - V_{COM}$$

$$V_{I(reg)} = V_I - V_O + V_{REF}$$

$$V_{I(reg)} = V_{DIFF} + V_{REF}$$

Since V_{REF} is fixed, the only limitation on the input voltage is the allowable differential voltage. This makes the adjustable regulator especially suited for high-voltage applications ($V_I > 40$ V).

Practical values of output voltage are limited to practical ratios of output-to-reference voltages.

$$\frac{R2}{R1} = \frac{V_O}{V_{REF}} - 1$$

The adjustable regulator exhibits power consumption characteristics similar to that of the series regulator from which it is derived.

Current Regulator

The adjustable regulator can also serve as a constant current regulator as shown in Figure 5–19.

$$I_L = I_O = \frac{V_{O(reg)}}{R_S} = \frac{V_{REF}}{R_S}$$
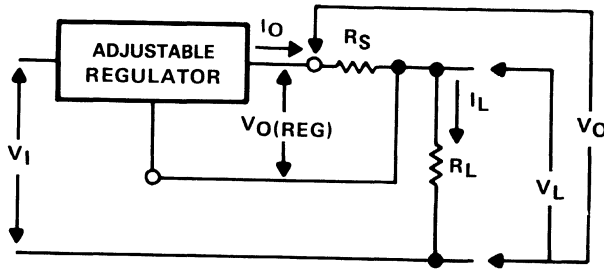
Fig. 5–19   Adjustable Regulator as a Constant-Current Regulator.

Shunt Regulator

The shunt regulator, illustrated in Figure 5–20, is the simplest of all regulators. It employs a fixed resistor as its series pass element.
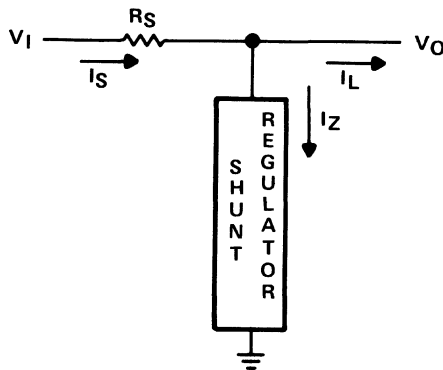
Fig. 5–20   Shunt Regulator.

Changes in input voltage or load current requirements are compensated by modulating the current which is shunted to ground through the regulator.

For changes in V_I: $\Delta I_Z = \dfrac{\Delta V_I}{R_S}$

For changes in I_L: $\Delta I_Z = -\Delta I_L$

The inherent short-circuit-proof feature of the shunt regulator makes it particularly attractive for some applications. The output voltage will be maintained until the load current required is equal to the current through the series element (see Figure 5–21).

$I_L = I_S;\ (I_Z = 0)$
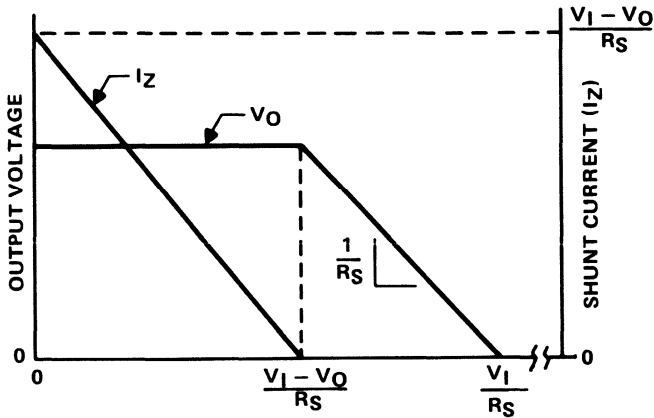
Fig. 5–21   Output Voltage vs Shunt Current of a Shunt Regulator.

Since the shunt regulator cannot supply any current, additional current required by the load will result in reducing the output voltage to zero.

$V_O = V_I - I_L R_S$

The short-circuit current of the shunt regulator then becomes:

$V_O = 0$

$I_{SC} = \dfrac{V_I}{R_S}$

Switching Regulators

The switching regulator lends itself primarily to the higher power applications or those applications where power supply and system efficiency are of the utmost concern. Above approximately 25 watts output power the cost of a switching regulator design will usually be lower than a series or shunt solution. However, when factors such as size, weight, input voltage range, etc, are taken into account switching designs can be beneficial at much lower power levels.

Unlike the series regulator, the switching regulator operates its control element in an on or off mode. Switching regulator control element modes are illustrated in Figure 5–22.
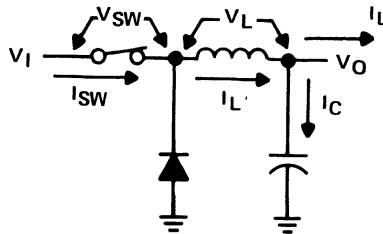
(a) ON-STATE

$$P_{SW} = V_{SW} I_{SW}$$
$$V_{SW} = 0 \text{ V}$$
$$P_{SW} = 0 \text{ W}$$
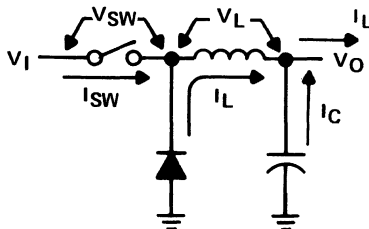
(b) OFF-STATE

$$P_{SW} = V_{SW} I_{SW}$$
$$I_{SW} = 0 \text{ A}$$
$$P_{SW} = 0 \text{ W}$$

Fig. 5–22   Switching Voltage Regulator Modes

In this manner, the control element is subjected to a high current at a very low voltage or a high differential voltage at a very low current. In either case, power dissipation in the control element is minimal. Changes in the load current or input voltage are compensated for by varying the on-off ratio (duty cycle) of the switch without increasing the internal power dissipated in the switching regulator. See Figure 5–23(a).

(a)

(b)
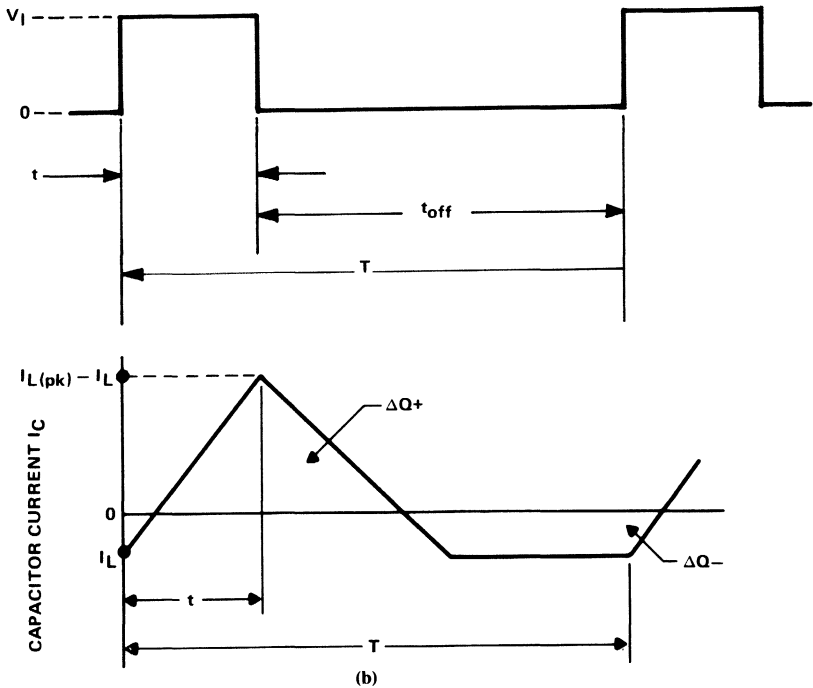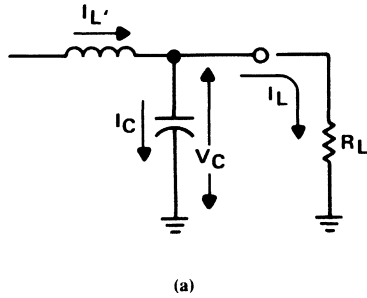
Fig. 5–23   Variation of Pulse Width vs. Load.

For the output voltage to remain constant, the net charge in the capacitor must remain constant. This means the charge delivered to the capacitor must be dissipated in the load.

$$I_C = I_L' - I_L$$

$$I_C = I_L' \text{ for } I_L = 0$$

$$I_C = I_{L(pk)} - I_L \text{ for } I_L' = I_{L(pk)}$$

The capacitor current waveform then becomes that illustrated in Figure 5–23(b). The charge delivered to the capacitor and the charge dissipated by the load are equal to the areas under the capacitor current waveform.

$$\Delta Q+ = \frac{1}{2} \frac{(I_{L(pk)} - I_L)^2}{I_{L(pk)}} t\left(\frac{V_I}{V_C}\right)$$

$$\Delta Q- = I_L\left[T - \frac{1}{2}t\left(\frac{V_I}{V_C}\right)\right.$$

$$\left. - \frac{1}{2}t\left(\frac{I_{L(pk)} - I_L}{I_{L(pk)}}\right)\left(\frac{V_I}{V_C}\right)\right]$$

By setting $\Delta Q+$ equal to $\Delta Q-$, the relationship of I_L and $I_{L(pk)}$ for $\Delta Q = 0$ can be determined:

$$I_L = \frac{1}{2}I_{L(pk)}\left[\frac{V_I}{V_C}\frac{t}{T}\right]$$

As this demonstrates, the duty cycle t/T can be altered to compensate for input voltage changes or load variations.

The duty cycle t/T can be altered a number of different ways.

$t = t_{on}$ (inductor charge time)

$T = $ Total time ($t_{on} + t_{off}$)

Fixed-Frequency, Variable Duty Cycle (PWM)

The most popular switching regulator configuration is fixed-frequency where the duty cycle of the pulse train is varied in order to change the average power. The fixed-frequency concept is particularly advantageous for systems employing transformer-coupled output stages. The fixed frequency permits efficient design of the associated magnetics. Transformer coupling also has advantages in single and multiple voltage-conversion applications. The fixed-frequency regulator will establish a dc current through the inductor (for increased load conditions) to maintain the required load current, with minimal ripple current. The single-ended and transformer-coupled configurations are illustrated in Figure 5–24.

STEP-DOWN   STEP-UP   INVERT

(a) SINGLE-ENDED CONFIGURATIONS

FLYBACK   PUSH-PULL

(b) TRANSFORMER-COUPLED CIRCUITS
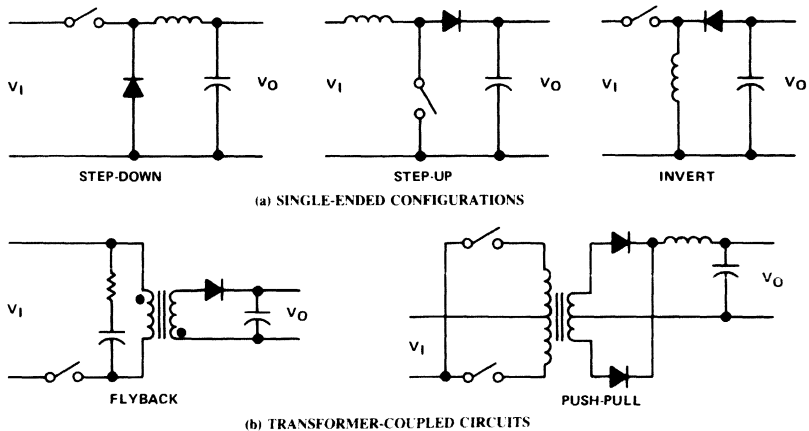
Fig. 5–24   Switching Voltage Regulator Configurations.

These types of switching regulators can thus be operated with high efficiency to provide low-voltage, regulated outputs from a high-voltage, unregulated supply or vice versa. The switching frequency should be established at the optimum value for the switching components of the supply (transformer, switching transistor, inductor, and filter capacitor). High frequency operation is distinctly advantageous because the cost, weight, and volume of both L and C filter elements are reduced.

However, the frequency at which the effective series resistance of the filter capacitor equals its capacitive reactance is the maximum allowable frequency.

Operation above 20 kHz is desirable to eliminate the possibility of audible noise. Choosing an operating frequency that is too high will result in power switching transistor losses as well as 'catch' diode losses. The higher cost of these high performance components must be balanced against the reduced cost, size, and weight of the L and C components when determining the optimum frequency for a specific application.

Fixed On Time, Variable Frequency

Another technique of voltage regulation is to maintain a fixed or predetermined 'on' time (t) (the time the input voltage is being applied to the LC filter) and vary the duty cycle by varying the frequency (f). This method makes voltage conversion applications design easier (step-up, step-down, invert) since the energy stored in the inductor of the LC filter during the on-time (which is fixed) determines the amount of power deliverable to the load. Thus calculation of the inductor is fairly straightforward.

$$L = \frac{V}{I} t$$

where

   L = value of inductance in microhenrys

   V = differential voltage in volts

   I = required inductor current defined by the load in amps

   t = on-time in microseconds

The fixed-on-time approach is also advantageous from the standpoint that a consistent amount of energy is stored in the inductor during the fixed on-time period. This simplifies the design of the inductor by defining the operating parameters to which the inductor is subjected. The operating characteristic of a fixed-on-time switching voltage regulator is a varying frequency, which changes directly with changes in the load. This can be seen in Figure 5–25.
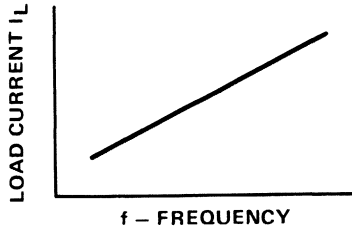
Fig. 5–25   Frequency vs Load Current for Fixed On-Time SVR.

THERMAL CONSIDERATIONS

Like any semiconductor circuit, lower operating temperature greatly improves reliability of a voltage regulator. It is good practice to make the input-to-output drop across a three-terminal regulator as low as possible while maintaining good regulation. Larger voltage drops mean more power dissipated in the regulator. Although most regulators are rated to withstand junction temperatures as high as 150°C, heat sinking should be provided to maintain the lowest possible temperature.

REGULATOR SAFE OPERATING AREA

The safe operating area (SOA) is a term used to define the input and output voltage range, and load current range within which any device is designed to operate reliably. Exceeding these limits will result in a catastrophic failure or will render the device temporarily inoperative, depending upon the device and its performance characteristics. Integrated circuit voltage regulators with internal current limiting, thermal and short-circuit protection will merely shut down. External components, such as pass transistors on the other hand, may respond with catastrophic failure.

Regulator Safe Operating Area Considerations

Although particular design equations depend upon the type of integrated circuit voltage regulator used and its application, there are several boundaries that apply to all regulator circuits for safe, reliable performance.

Input Voltage

The limits on the input voltage are derived from three considerations:

V_{Imax}
The absolute maximum rated input voltage as referenced to the regulator's ground. This is a safe operating area (SOA) destruct limit.

$(V_I - V_O)_{min}$
The input-to-output differential voltage, also referred to as the dropout voltage, at which the regulator ceases to function properly. This is a functional limit.

$(V_I - V_O)_{max}$
The maximum input-to-output differential voltage. Usually, the regulator's power dissipation is exceeded prior to the $(V_I - V_O)_{max}$ limit. This is an SOA level that can be limited by the allowable Power Dissipation (P_{Dmax}).

Load Current

I_{Lmax}
The maximum load current deliverable from the integrated circuit regulator. If internal current limiting is not provided, external protection should be provided. This is a functional limit that may be further limited by P_{Dmax}.

Power Dissipation

P_{Dmax}
The maximum power that can be dissipated within the regulator. Power dissipation is the product of the input-to-output differential voltage and the load current, and is normally specified at or below a given case temperature. This rating is usually based on a 150°C junction temperature limit. The power rating is an SOA limit unless the integrated circuit regulator provides internal thermal protection.

Output Voltage of an Adjustable-Voltage Regulator

V_{Omin}
> The minimum output voltage a regulator is capable of regulating. This is usually a factor of the regulator's internal reference and is a functional limit.

V_{Omax}
> The maximum output voltage a regulator is capable of regulating. This is largely dependent on the input voltage and is a functional limit.

External Pass Transistor

For applications requiring additional load current, integrated circuit voltage regulator capabilities may be boosted with the addition of an external pass transistor. When employed, the external pass transistor, in addition to the voltage regulator, must be protected against operation outside its safe operating area. Operation outside the safe operating area is catastrophic to most discrete transistors.

I_{Cmax}
> The maximum current the transistor is capable of sustaining. I_{Cmax} now becomes the maximum current the regulator circuit is capable of delivering to the load. Associated with I_{Cmax} is a collector-emitter voltage ($V_{CE} = V_I - V_O$). If the product $[V_I - V_{Omax}]I_{Cmax}$ exceeds the SOA then I_{Cmax} will have to be derated. This will then become a functional limit instead of a catastrophic limit. I_{Cmax} is related to power dissipation and junction or case temperature. I_{Cmax} must again be derated if the thermal or power ratings at which it is specified are exceeded. The resulting derated I_{Cmax} should continue to be considered as a catastrophic limit. Actual I_{Cmax} limits and derating information will appear on the individual transistor specification.

V_{CEmax}
> The maximum collector-emitter voltage that can be applied to the transistor in the off-state. Exceeding this limit can be catastrophic.

P_{Dmax}
> The maximum power than can be dissipated by the transistor. This is usually specified at a specific junction or case temperature. If the transistor is operated at higher temperatures, the

maximum power must be derated in accordance with the operating rules specified in the transistor's applicable specification. Prolonged operation above the transistor's maximum power rating will result in degradation or destruction of the transistor.

Safe Operating Protection Circuits

Selection of the proper integrated circuit voltage regulators and external components will result in a reliable design in which all devices can operate well within their respective safe operating areas. Fault conditions (such as a short-circuit or excessive load) may cause components in the regulator circuit to exceed their safe operating area. Because of this situation, as well as protection for the load, certain protection circuits should be considered.

Reverse Bias Protection

A potentially dangerous condition may occur when a voltage regulator becomes reverse biased. For example, if the input supply were crowbarred to protect either the supply itself or additional circuitry, the filter capacitor at the output of the regulator circuit would maintain the regulator's output voltage and the regulator circuit would be reverse biased. If the regulated voltage is large enough (greater than 7 V), the regulator circuit may be damaged. To protect against this, a diode can be used as illustrated in Figure 5–26.
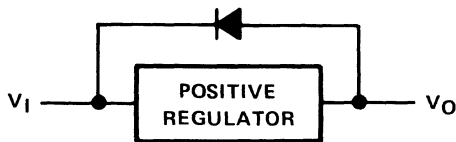
Fig. 5–26   Reverse Bias Protection.

Current Limiting Techniques

The type of current limiting used depends primarily on the safe operating area of the pass element used. The three basic current limiting techniques are series resistor, constant current, and fold-back current limiting.

Series Resistor

This is the simplest method for short-circuit protection. The short-circuit current is determined by the current-limiting resistor R_{CL}, illustrated in Figure 5-27.

$$V_O = V_{O(reg)} - I_L R_{CL}$$

A short-circuit condition occurs when $V_O = 0$, thus:

$$I_{SC} = I_L \ @ \ (V_O = 0) = \frac{V_{O(reg)}}{R_{CL}}$$
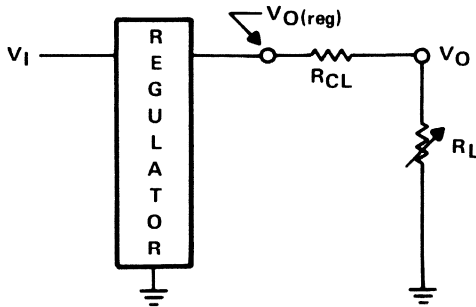
Fig. 5-27   Series resistance Current Limiter.

The primary drawback of this technique is error introduced by the voltage dropped across R_{CL} under varying load conditions. The % error, as illustrated by the following equations, depends on the R_{CL} and R_L values.

$$I_L = \frac{V_O}{R_L}$$

$$V_O = \frac{V_{O(reg)}}{1 + \dfrac{R_{CL}}{R_L}}$$

$$\% \ ERROR = \frac{V_{O(reg)} - V_O}{V_{O(reg)}}$$

$$\% \ ERROR = \frac{R_{CL}}{R_L + R_{CL}}$$

Maintaining R_{CL} at a level which is an order of magnitude less than the nominal load impedance minimizes this effect.

$$R_{CL} = \frac{1}{10} R_L \qquad \% \text{ ERROR} = 9.1\%$$

This also yields a short-circuit current that is an order of magnitude greater than the normal operating load current.

$$I_{L(norm)} = \frac{V_{O(reg)}}{R_{CL} + R_{L(norm)}}$$

$$I_{SC} = \frac{V_{O(reg)}}{R_{CL}}$$

$$I_{SC} = 11 \, I_{L(norm)}$$

This technique is obviously inefficient since it requires using a regulator or pass element with current capabilities in excess (11X) of its normal operating capabilities.

The performance characteristics of a series resistance current limited regulator are illustrated in Figure 5–28.
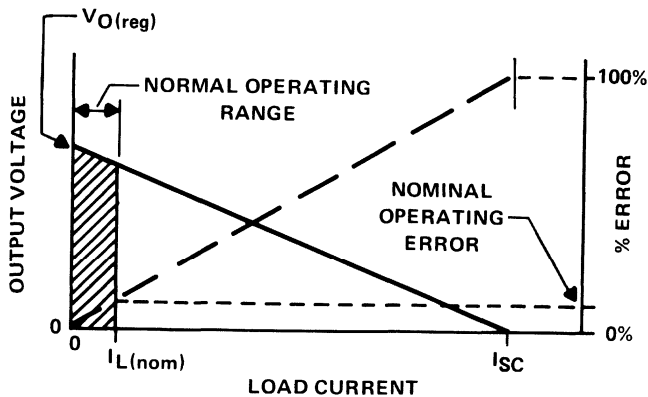
Fig. 5–28   Performance Characteristics of a Series Resistance Current-Limited Regulator.

Constant-Current Limiting

Constant-current limiting is the most popular current-limiting technique in low-power, low-current regulator circuits. The basic configuration is illustrated in Figure 5–29.

Fig. 5–29   Constant Current Limit Configuration.

Note that this method requires access to the control element and remote voltage sense capabilities. By sensing the output voltage beyond the current limiting resistor, the circuit allows the regulator to compensate for the voltage changes across R_{CL}.

If an external pass transistor is used, its base current may be starved to accomplish constant-current limiting, as illustrated in Figure 5–30.

Fig. 5–30   Constant Current Limiting for External Pass Transistor Applications.

Current limiting takes effect as the voltage drop across R_{CL} approaches the potential required to turn on transistor Q1. As Q1 is biased on, the current supplying the base of Q2 is diverted, thus decreasing the drive current to Q3, the regulator's pass transistor. The performance characteristics of a constant-current limited regulator are illustrated in Figure 5–31.
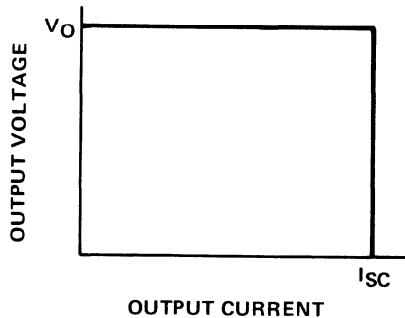
Fig. 5–31   Constant Current Limiting.

It should be noted that short-circuit conditions are the worst conditions that can be imposed on the pass transistor since it has to survive not only the short-circuit current, but it has to withstand the full input voltage across its collector and emitter terminals.

This normally requires the use of a pass transistor with power handling capabilities much greater than those required for normal operation i.e.:

$V_I = 20$ V $V_O = 12$ V $I_O = 700$ mA

NOMINAL $P_D = (20$ V $- 12$ V$) \times 0.7$ A $= 5.6$ W

For $I_{SC} = 1$ A(150% I_{OUT}):

SHORT-CIRCUIT $P_D = 20$ V $\times 1$ A $= 20$ W

This requirement may be reduced by the application of fold-back current limiting.

Fold-Back Current Limiting

Fold-back current limiting is used primarily for high-current applications where the normal operating requirements of the regulator dictate the use of an external power transistor. The principle of fold-back current limiting provides limiting at a predetermined current (I_K). At this predetermined current, feedback reduces the load current as the load continues to increase (R_L decreasing) and causes the output voltage to decay.
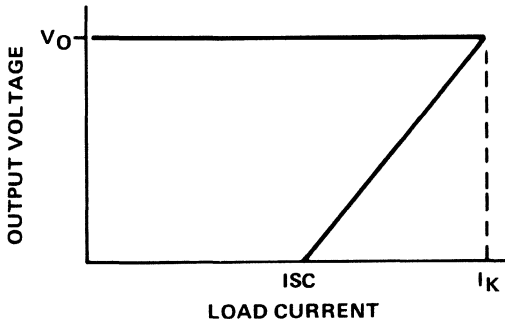
Fig. 5-32   Fold-Back Current Limiting.

The fold-back current-limiting circuit of Figure 5-33 behaves in a manner similar to the constant-current limit circuit illustrated in Figure 5-30. In Figure 5-33, the potential developed across the current limit sense resistor (R_{CL}) must not only develop the base-emitter voltage required to turn on Q1, but it must develop sufficient potential to overcome the voltage across the resistor R1.

$$V_{BE(Q1)} = R_{CL}I_L - \frac{V_O + R_{CL}I_L}{R1 + R2} \times R1$$

$$\therefore I_K = \frac{V_{BE(Q1)}(R1 + R2) + V_OR1}{R_{CL}R2}$$

As the load current requirement increases above I_K, the output voltage (V_O) decays. The decreasing output voltage results in a proportional decrease in voltage across R1. Thus, less current is required through R_{CL} to develop sufficient potential to maintain the forward-biased condition of Q1. This can be seen in the above

expression for I_K. As V_O decreases, I_K decreases. Under short-circuit conditions ($V_O = 0$), I_K becomes:

$$I_{SC} = I_K @ (V_O = 0) = \frac{V_{BE(Q1)}}{R_{CL}}\left[1 + \frac{R1}{R2}\right]$$
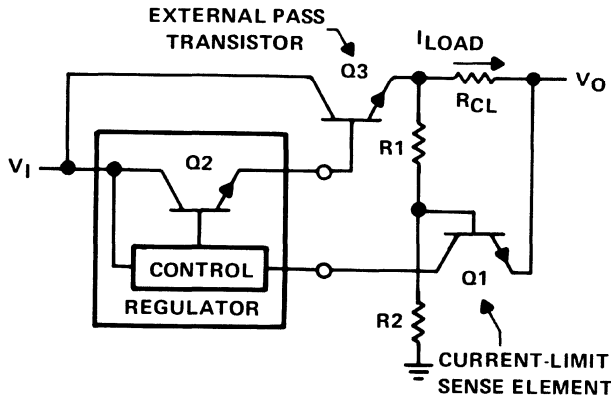
Fig. 5–33   Fold-Back Current Limit Configuration.

The approach illustrated in Figure 5–33 allows a more efficient design because the collector current of the pass transistor is less during short-circuit conditions than it is during normal operation. This means that during short-circuit conditions, when the voltage across the pass transistor is maximum, the collector-emitter current is reduced. As illustrated in Figure 5–34, fold-back current limiting fits closer to the
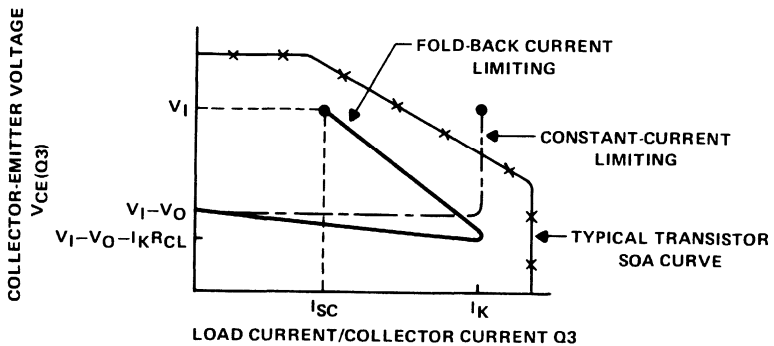
Fig. 5–34   Fold-Back Current Limit Safe Operating Area.

typical performance characteristics of the transistor, thus allowing a better design match of the pass transistor to the regulator.

LAYOUT GUIDELINES

Component layout and orientation plays an important, but often overlooked, role in the overall performance of the regulator. The importance of this role depends upon such things as power level, the type of regulator, the overall regulator circuit complexity, and the environment in which the regulator operates. The general layout rules, as well as remote voltage sensing, and component layout guidelines are discussed in the following text.

Layout Design Factors

Most integrated circuit regulators use wide-band transistors to optimize their response. These regulators must be compensated to ensure stable closed-loop operation. This compensation can be counteracted by a layout which has excess external stray capacitance and line inductance. For this reason, circuit lead lengths should be held to a minimum. Lead lengths associated with external compensation capacitors or pass transistor elements are of primary concern. These components especially, should be located as close as possible to the regulator control circuit. In addition to affecting a regulator's susceptibility to spurious oscillation, the layout of the regulator also affects its accuracy and performance.

Input Ground Loop

Improper placement of the input capacitor can induce unwanted ripple on the output voltage. Care should be taken to ensure that currents in the input circuit do not flow in the ground line that is in common with the load return. This would cause an error voltage resulting from the peak currents of the filter capacitor flowing through the line resistance of the load return. See Figure 5–35 for an illustration of this effect.

(a) TYPICAL LAYOUT

(b) LAYOUT ERROR CONTRIBUTIONS
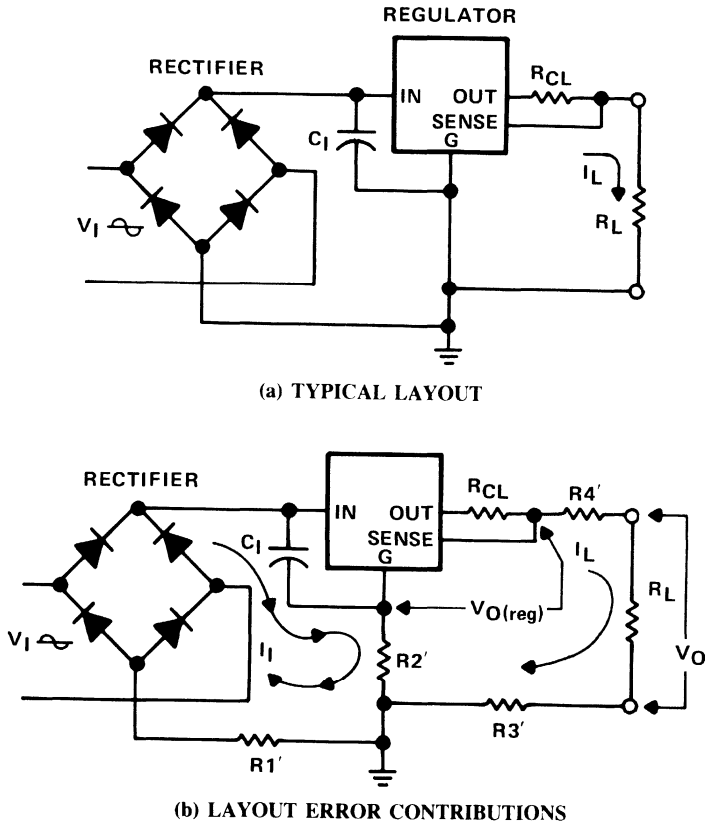
Fig. 5-35   Circuit Layout Showing Error Contributions.

Output Ground Loop

Similar in nature to the problem discussed on the input, excessive lead length in the ground return line of the output results in additional error. Because the load current flows in the ground line, an error equivalent to the load current multiplied by the line resistance (R3') will be introduced in the output voltage.

Remote Voltage Sense

The voltage regulator should be located as close as possible to the load. This is true especially if the output voltage sense circuitry is

internal to the regulator's control device. Excessive lead length will result in an error voltage developed across the line resistance (R4′).

$$V_O = V_{O(reg)} - (R_2' + R_3' + R_4') I_L + R2'I_{reg}$$

$$ERROR = I_L(R_3' + R_4') - I_{Ireg}R_2'$$

If the voltage sense is available externally, the effect of the line resistance can be minimized. By referencing the low current external voltage sense input to the load, losses in the output line are compensated. Since the current in the sense line is very small, error introduced by its line resistance is negligible (Figure 5–36).
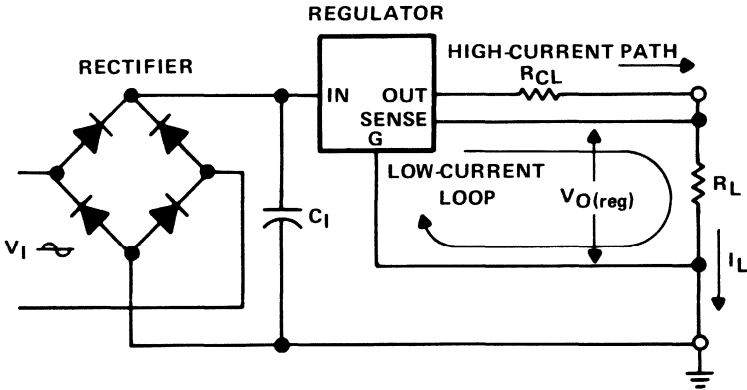
Fig. 5–36   Proper Regulator Layout.

Thermal Profile Concerns

All semiconductor devices are affected by temperature; therefore, care should be taken to the placement of these devices so that their thermal properties are not additive. This is especially important where external pass transistors or reference elements are concerned.

INPUT SUPPLY DESIGN

When the power source is an ac voltage, the transformer, rectifier, and input filter design are as important as the regulator design itself for optimum system performances. This section presents input supply and filter design information for designing a basic capacitor input supply.

Transformer/Rectifier Configuration

The input supply consists of three basic sections: (1) input transformer, (2) rectifier, and (3) filter as illustrated in Figure 5–37.
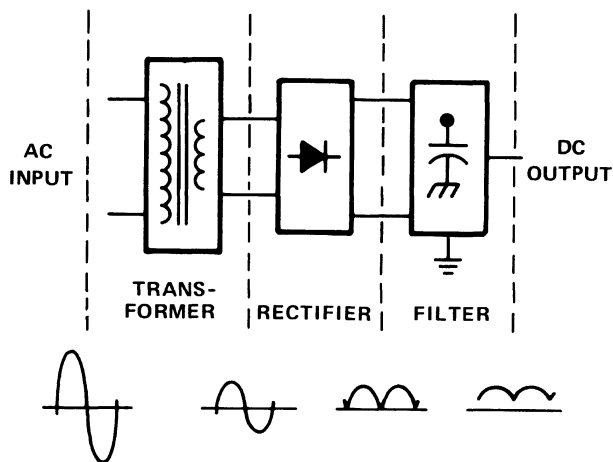
Fig. 5–37   Input Supply.

The first two sections, the transformer and the rectifier, are partially dependent upon each other because the structure of one depends upon that of the other. The most common transformer configurations and their associated rectifier circuits are illustrated in Figure 5–38.

The particular configuration used depends upon the application. The half-wave circuit [Figure 5–38(a)] is used in low-current applications. This is because the single rectifier diode experiences the total load current and its conversion efficiency is less than 50%. The full-wave configurations [Figures 5–38(b) and 5–38(c)] are used for higher current applications. The characteristic output voltage waveforms of these configurations are illustrated in Figure 5–39.

Before the input supply and its associated filter can be designed, the voltage, current, and ripple requirements of its load must be fully defined. The load, as far as the input supply is concerned, is the regulator circuit. Therefore, the input requirements of the regulator itself become the governing conditions.

(a) SINGLE-PHASE HALF-WAVE

(b) SINGLE-PHASE CENTER-TAPPED FULL-WAVE

(c) SINGLE-PHASE FULL-WAVE BRIDGE
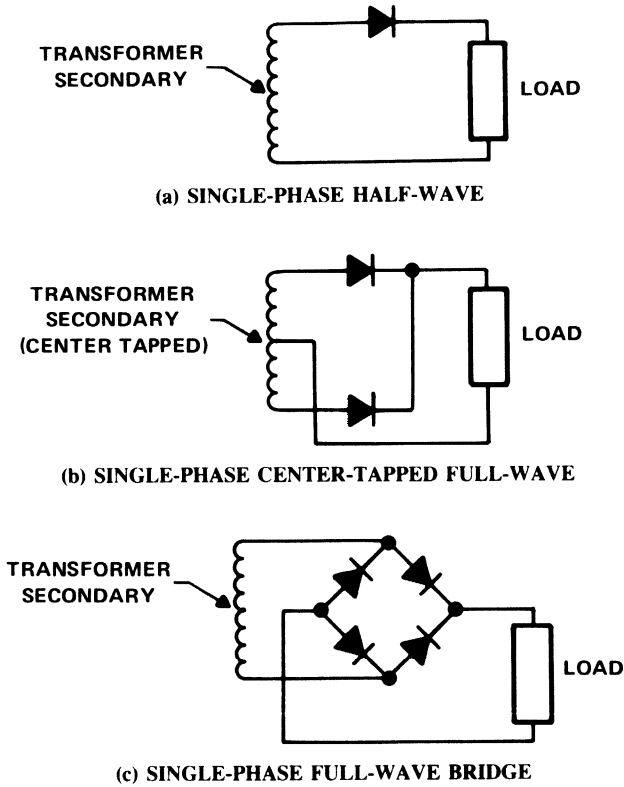
Fig. 5–38   Input Supply Transformer/Rectifier Configurations.
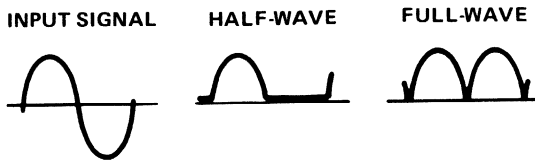
Fig. 5–39   Rectifier Output-Voltage Waveforms.

Because the input requirements of the regulator control circuit govern the input supply and filter design, it is easiest to work backwards from the load to the transformer primary.

Capacitor Input Filter Design

The most practical approach to a capacitor-input filter design remains the graphical approach presented by O.H. Schade[1] in 1943. The curves illustrated in Figure 5–40 through 5–43 contain all of the design information required for full-wave and half-wave rectifier circuits.
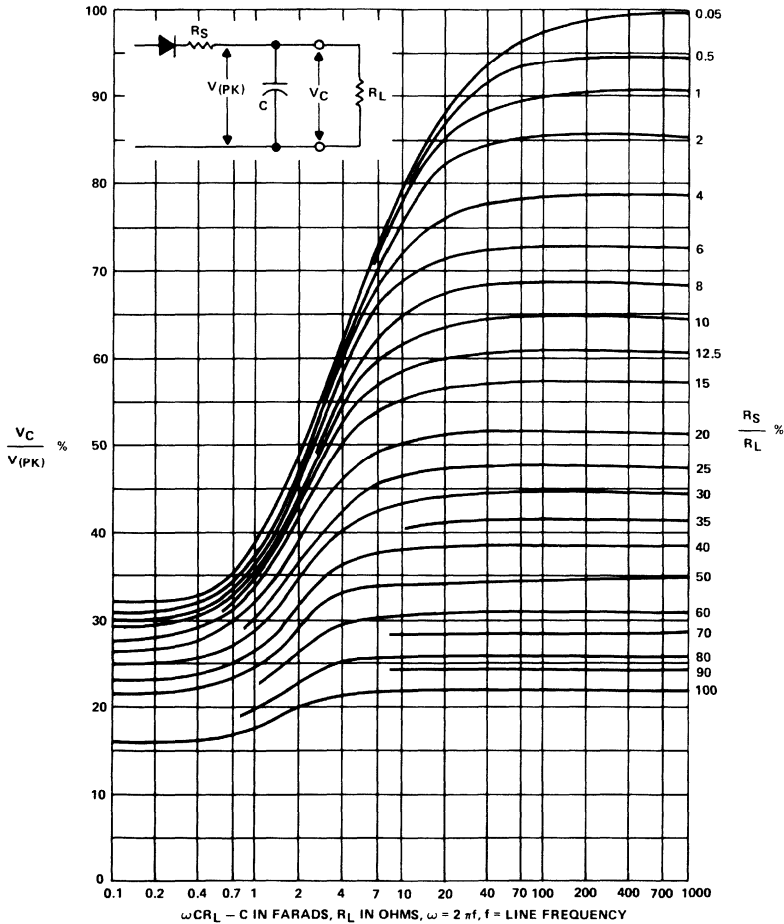
Fig. 5–40   Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Half-Wave Capacitor-Input Circuits (From O.H. Schade, Proc. IRE, Vol. 31, p. 343, 1943).

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[1] O.H.Schade, 'Analysis of Rectifier Operation', *Proc. IRE.*, VOL. 31, 343, 1943.

Figures 5–40 and 5–41 illustrate the ratio of the dc output voltage developed (V_C), to the applied peak input voltage ($V_{(PK)}$), as a function of ωCR_L, for half-wave and full-wave rectified signals respectively. For a full-wave rectified application, the voltage reduction is less than 10% for $\omega CR_L > 10$ and $R_S/R_L < 0.5\%$. As illustrated, the voltage reduction decreases as ωCR_L increases or the R_S/R_L ratio decreases. Minimizing the reduction rate, contrary to initial impressions, may prove to be detrimental to the optimum circuit design. Further reduction requires a reduction in the series to load resistance ratio (R_S/R_L) for any given ωCR_L. This will result in a higher peak-to-average current ratio through the rectifier diodes (see Figure 4–42). In addition, and probably of more
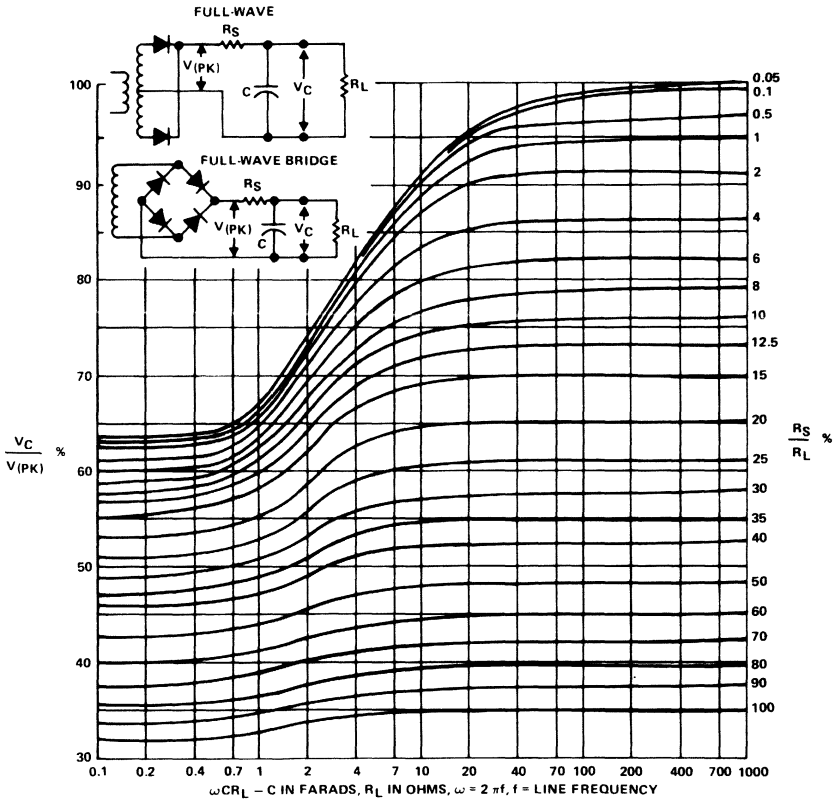
Fig. 5–41   Relation of Applied Alternating Peak Voltage to Direct
Output Voltage in Full-Wave Capacitor-Input Circuits (From O.H.
Schade, Proc. IRE, Vol. 31, p. 344, 1943).

concern, this increases the surge current experienced by the rectifier diodes during turn-on of the supply. It is important to realize that the surge current is limited only by the series resistance R_S.

$$I_{SURGE} = \frac{V_{SEC(PK)}}{R_S}$$

In order to control the surge current, additional resistance is often required in series with each rectifier. It is evident that a compromise must be made between the voltage reduction and the rectifier current ratings.

n = 1 (FOR HALF-WAVE SINGLE PHASE RECTIFIER CIRCUITS) or
n = 2 (FOR FULL-WAVE SINGLE PHASE RECTIFIER CIRCUITS)
ω = 2 πf = LINE FREQUENCY

C IN FARADS
R_L IN OHMS
R_S = RMS EQUIVALENT
        SOURCE RESISTANCE
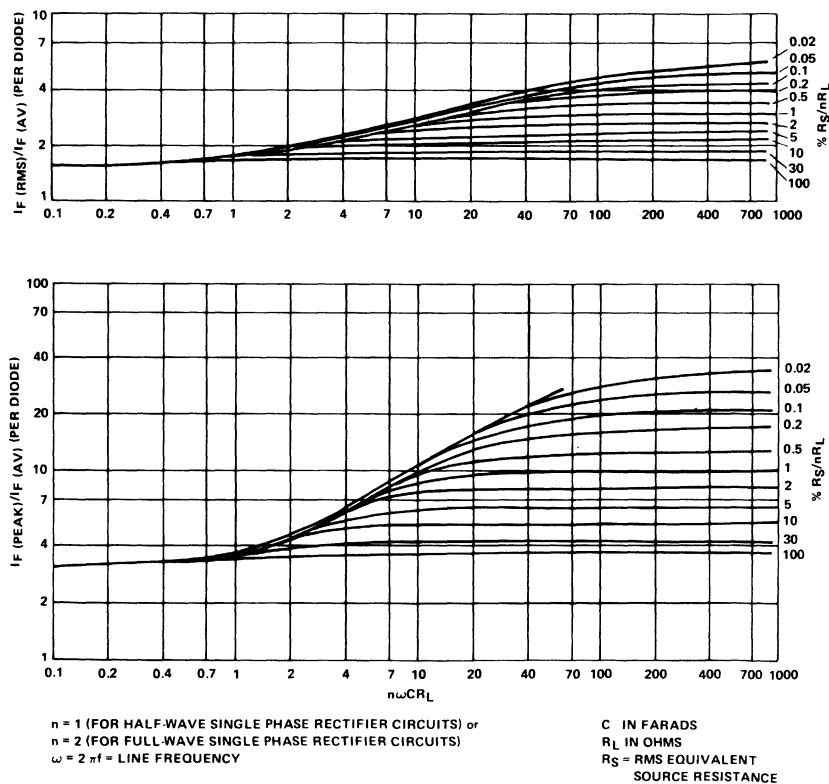
Fig. 5–42   Relation of RMS and Peak to Average Diode Current in Capacitor Input Circuits (From O.H. Schade, Proc. IRE, *Vol. 31, p. 345, 1943).*

The maximum instantaneous surge current is $V_{(pk)}/R_S$. The time constant (τ) of capacitor C is:

$$\tau \cong R_S C$$

As a rule of thumb, the surge current will not damage the diode if:

$$I_{SURGE} < I_{F(SURGE)max} \text{ and } \tau < 8.3 \text{ ms}$$

Figure 5-43 illustrates the relationships between the ripple factor r_f, $\omega C R_L$, and R_S/R_L. The ripple factor is the ratio of the rms value of the ripple component of the output voltage, expressed as a percent of the nominal dc output voltage.
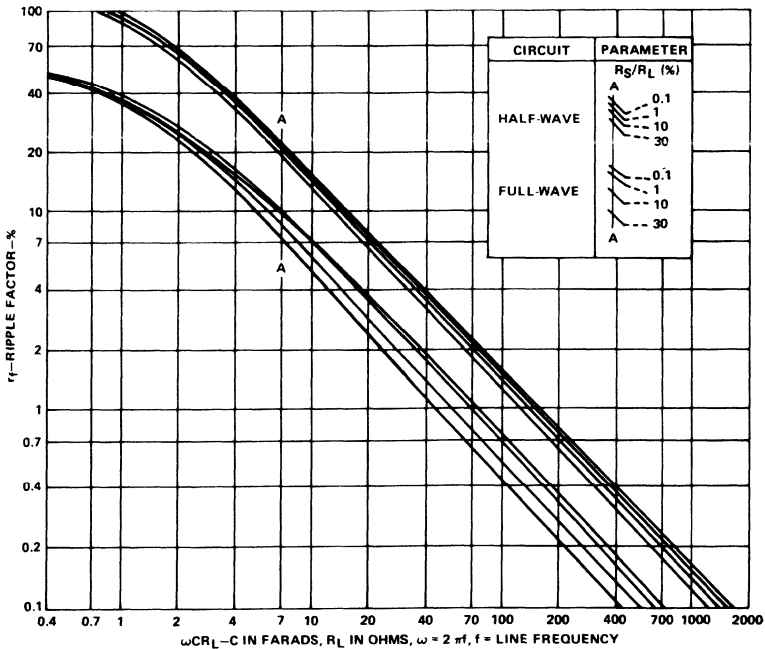
<i>Fig. 5-43   Root-Mean-Square Ripple Voltage for Capacitor-Input Circuits (From O.H. Schade,</i> Proc. IRE, <i>Vol. 31, p. 346, 1943).</i>

DEVICE APPLICATION EXAMPLES

THREE TERMINAL REGULATORS

Three-terminal IC regulators have been especially useful to the designer of small, regulated power supplies or on-card regulators. Three-terminal regulators are popular because they are small and require a minimum number of external components.

Stabilization

Mounting and using three-terminal regulators usually presents no problem, however, there are several precautions that should be observed. Positive regulators, in general, use npn emitter follower output stages, whereas negative regulators use npn common-emitter stages with the load connected to the collector. The emitter follower output stage configuration is not used in negative regulators because monolithic pnp series-pass transistors are more difficult to make. Due to their output stage configuration, positive regulators are more stable than negative regulators. Therefore, the practice of bypassing positive regulators may be omitted in some applications. It is good practice, however, to use bypass capacitors at all times.

For a positive regulator, a 0.33 μF bypass capacitor should be used on the input terminals. While not necessary for stability, an output capacitor of 0.1 μF may be used to improve the transient response of the regulator. These capacitors should be on or as near as possible to the regulator terminals. See Figure 5–44.
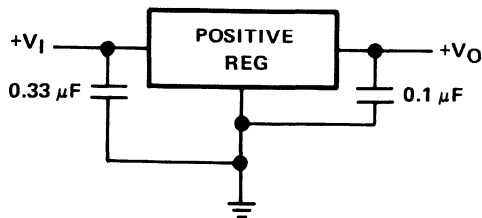
Fig. 5–44   Positive Regulator.

When using a negative regulator, bypass capacitors are a must on both the input and output. Recommended values are 2 μF on the input and 1 μF on the output. It is considered good practice to include an additional 0.1 μF capacitor on the output to improve the transient response (Figure 5-45). These capacitors may be mylar, ceramic, or tantalum, provided that they have good high frequency characteristics. A good combination is electrolytic bypass capacitors and a small ceramic capacitor.
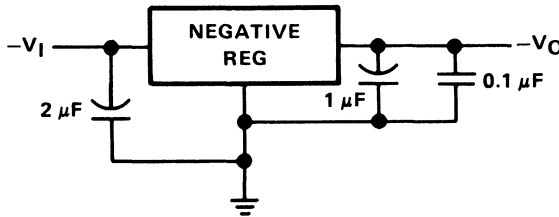
Fig. 5-45   Negative Regulator.

Fixed Dual Regulators

When building a dual power supply with both a positive and a negative regulator, extra precautions should be taken. If there is a common load between the two supplies, latch-up may occur. Latch-up occurs because a three-terminal regulator does not tolerate a reverse voltage of more than one diode drop. To prevent this latch-up problem it is good design practice to place reversed-biased diodes across each output of a dual supply. While the diodes should not be necessary if the dual regulator outputs are referenced to ground, latch-up may occur at the instant power is turned on, especially if the input voltage to one regulator rises faster than the other. This latch-up condition usually affects the positive regulator rather than the negative regulator. These diodes prevent reverse voltage to the regulator and prevent parasitic action from taking place when the power is turned on. The diodes should have a current rating of at least half the output current. A recommended circuit for a dual 15 V regulated supply is illustrated in Figure 5-46.

In Figure 5–46, 1N4001 diodes are placed directly across the regulators, input to output. When a capacitor is connected to the regulator output, if the input is shorted to ground, the only path for discharging the capacitor normally is back through the regulator. This could be (and usually is) destructive to the regulator. The diodes across the regulator divert any discharge current, thus protecting the regulator.
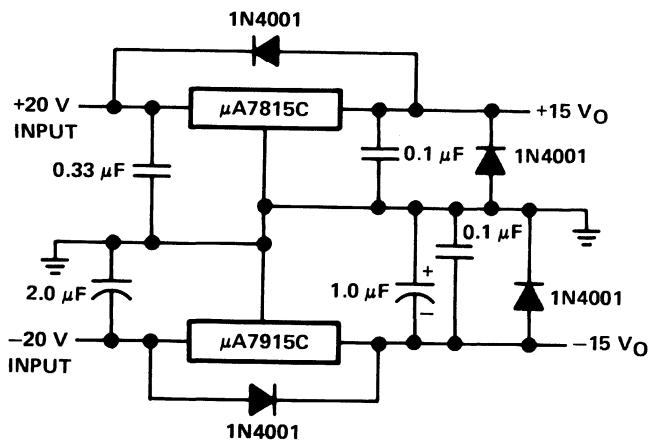
Fig. 5–46   Regulated Dual Supply.

Series Adjustable Regulators

Figure 5–47 illustrates a typical circuit for an LM317 adjustable positive regulator with the output adjustable from 1.2 V to 17 V and up to 1.5 A of current.
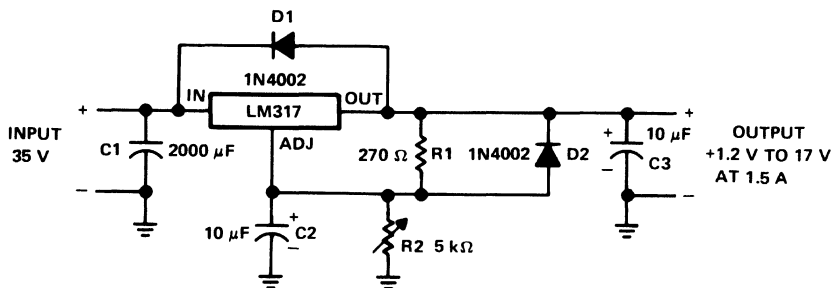
Fig. 5–47   Positive Adjustable Series Regulator.

Stabilization, as described earlier for fixed three-terminal regulators, is usually not required. Although the LM317 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This effect occurs with values between 500 pF and 5000 pF. Using a 10 μF aluminium electrolytic on the output swamps this effect and ensures stability.

C1 is the power supply filter capacitor following the rectifier section and should be connected close to the regulator input for maximum stability. If the input were to be shorted, D1 would divert the discharge current around the regulator, protecting it. Also, with both D1 and D2 in the circuit, when the input is shorted, C2 is discharged through both diodes. In general, a diode should be used in the position occupied by D1 on all positive regulators to prevent reverse biasing. This becomes more important at higher output voltages since the energy stored in the capacitors is larger. Bypassing the adjustment terminal (C2) improves ripple rejection. Output capacitor C3 is added to improve the transient response of the regulator.

In both the negative (LM337) and the positive (LM317) series adjustable regulators there is an internal diode from the input to the output. If the total output capacitance is less than 25 μF, D1 may be omitted.

ADJUSTABLE SHUNT REGULATOR TL430–TL431

The TL430 and TL431 are three-terminal 'programmable' shunt regulators. The devices are basically the same except the TL431 contains a diode connected between the emitter and collector of the output transistor. The standard symbol and block diagram are shown in Figure 5–48.

The circuit consists of a bipolar op-amp driving an npn transistor. The TL431 has a true temperature compensated band-gap reference and is more stable and accurate than other shunt regulators. The TL431 also has a diode across the emitter-collector of the npn output transistor. If the cathode goes negative, the diode conducts around the transistor, emulating the performance characteristics of a normal zener diode. The basic operating characteristics are shown in Figure 5–49.

TL430 — TL431

ANODE ———————— CATHODE

REF

(a) SYMBOL

CATHODE

REF

TL431 ONLY

ANODE

(b) BLOCK DIAGRAM
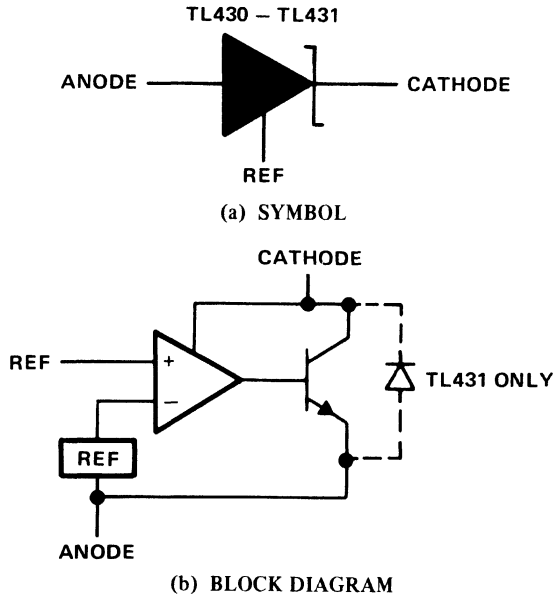
Fig. 5–48   TL430/TL431 Adjustable Shunt Regulators.

TL430, TL431 PROGRAMMABLE ZENERS

R_S

V_{IN}

V_Z

R1

V_{ref}

R2

TL431

4.7 V
ZENER
DIODE

mA

VOLTS/DIV
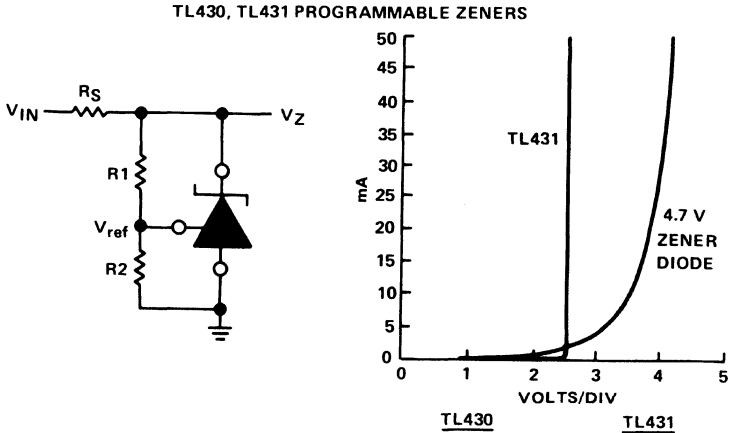
	TL430	TL431
• TEMPERATURE COMPENSATED	200 ppm/°C	100 ppm/°C
• LOW DYNAMIC IMPEDANCE	1.5 OHMS	0.2 OHMS
• TYPICAL V_{ref}	2.75 V	2.5 V
• REGULATES FROM 1.0 - 100 mA OVER ADJUSTABLE VOLTAGE RANGE	2.75-30 V	2.5-36 V

Fig. 5–49   Basic Operating Characteristics.

Their excellent thermal stability make these devices extremely attractive as a replacement for high cost temperature-compensated zeners. As seen in Figure 5–50, the TL431 offers improved characteristics, even at low voltages. As with all shunt regulators the TL431 can be used as either a positive or negative voltage reference. The TL431 has an equivalent full-range temperature coefficient of 50 ppm/°C (typical) and has low output noise voltage. Note in the graph (Figure 5–50) that for a nominl 2.495 V reference the curve is essentially flat from 0°C to 70°C.
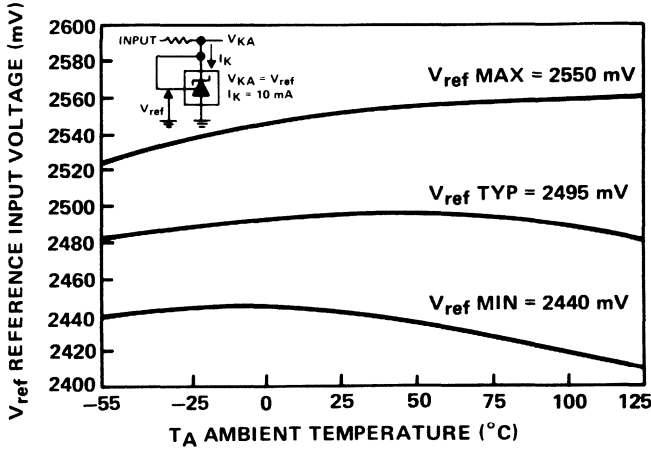
Fig. 5–50   Reference Voltage Versus Ambient Temperature.

Depending upon the zener voltage, the TL431 also has an extremely low dynamic impedance of about 0.2 Ω, compared to a standard zener diode's dynamic impedance of about 30 to 60 Ω.

$$V_Z = V_{REF} \left[1 + \frac{R1}{R2}\right]$$

$$V_{REF} = 2.5\ V$$
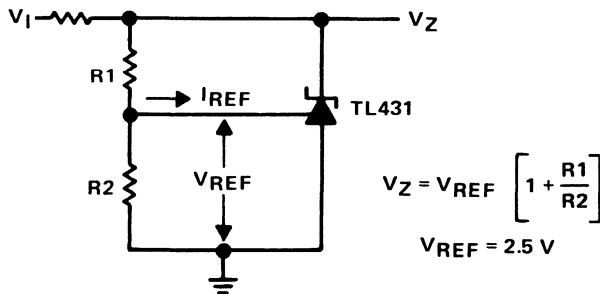
Fig. 5–51   Basic Operational Circuit.

A 2.5 V reference voltage is developed across R2 as shown in Figure 5–51. I_{ref}, the current input at the reference terminal, is about 10 μA. To maintain a steady reference, it is advisable to allow 1 mA of current flow through series resistors R1 and R2. This will assure a stable reference voltage independent of I_{ref} variations.

The circuit in Figure 5–35 uses a TL431 as a regulator to control the base drive to a TIP660 series pass transistor. For good reference stability, a current flow of about 1 mA (I_2) through the resistor divider is recommended. A 2.5 V reference voltage is developed across R2, and R1 will develop a voltage drop of 21.5 V. The Darlington power transistor is used because of the reduced base drive requirement of the TIP660 which has a V_{be} (max) of about 2 V. The h_{FE} at $I_C = 2.5$ A is about 1000, so it would only require about 2.5 mA of base drive to produce 2.5 A of output current.
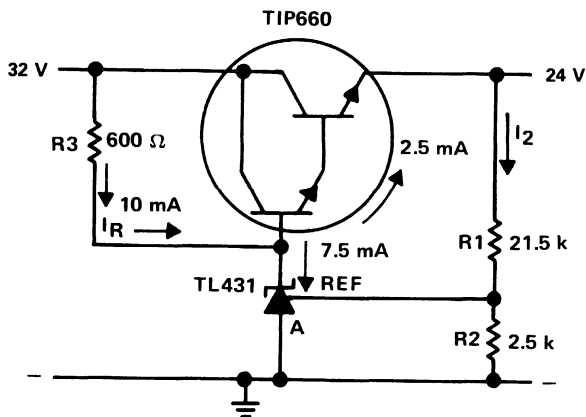
Fig. 5–52   Series Regulator Circuit.

Values for Figure 5–52 are calculated as follows:

$$R3 = \frac{V_I - (V_{be} + V_O)}{I_R}$$

$$R3 = \frac{32 - (2 + 24)}{10\,\text{mA}} = 600\,\Omega$$

$$V_O = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

R1 = 21.4 Ω

R2 = 2.5 kΩ

In calculating the value of the current limit resistor, R3, we assume about 7.5 mA of current through the TL431. The value of R3 is therefore 600 Ω and the current about 10 mA, so a 1/2 W resistor will suffice. This is a simple method of designing a medium output current power-supply using only four components plus the series pass transistor.

SHUNT REGULATOR APPLICATIONS

a) Crowbar

To protect solid-state electronic equipment from overvoltage due to a power-supply component failure, it is sometimes desirable to use a 'crowbar' circuit. When a preset voltage is exceeded, the SCR turns on, shorting the output and blowing the fuse on the input side of the crowbar circuit. The circuit in Figure 5–53 is set to trip when V_O reaches 27 V. When this occurs, the reference voltage input will be greater than 2.5 V. This will turn on the TL431 which then causes the pnp transistor to conduct by pulling its base low. This turns the SCR on and immediately blows the safety fuse on the circuit input, thus protecting the equipment using this power supply.

$$V_{LIMIT} = \left(1 + \frac{R1}{R2}\right)V_{REF}$$
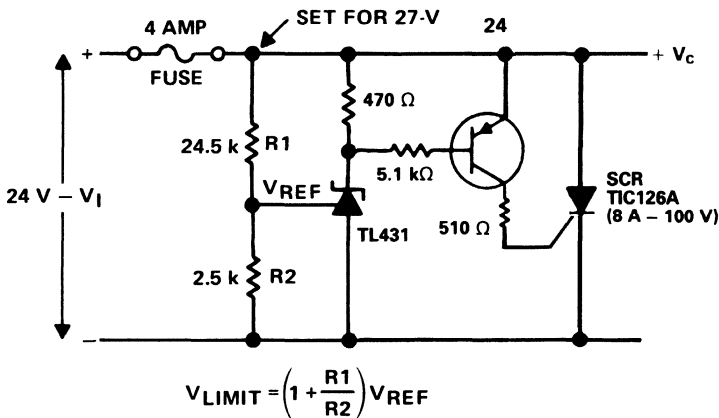
Fig. 5–53   Shunt Regulator in Crowbar Circuit.

b) Controlling V_O of a Fixed Output Voltage Regulator

Sometimes it is necessary to have a regulated output voltage different from that for which the regulator is designed. This may be accomplished with any three-terminal regulator, although it should be noted that the lowest obtainable voltage will be 2.5 V for the TL431 plus the voltage of the three-terminal regulator. In the circuit in Figure 5–54, the lowest possible regulated voltage would be 7.5 V (2.5 V for the TL431 + 5 V for the 7805). This particular circuit provides 9 V output using a uA7805 three-terminal regulator.
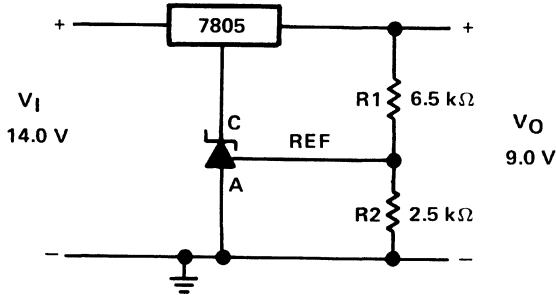
NOTE: MINIMUM $V_O = V_{REF} + 5.0$ V

$$V_O = \left(1 + \frac{R1}{R2}\right) V_{REF}$$

Fig. 5–54   Fixed Output Shunt Regulator.

c) Current Limiter

Figure 5–55 is an example of a current limiter designed to limit the current from a 12 V supply to 1.5 A using a TIP31 npn transistor as the pass element. The value of R1 is calculated from the equation in Figure
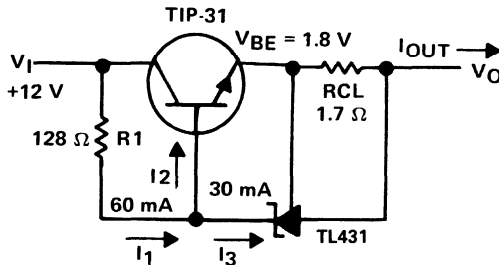
Fig. 5–55   Current Limiter.

5–55. The current through R1 is split almost equally in this circuit, with about 30 mA going to the TL431, and 30 mA for base drive to the TIP31. With a current load of 60 mA, and an R1 value of 128 Ω a 1/2 watt resistor is sufficient. When the voltage across the current limit resistor (R_{CL}) reaches 2.5 V (TL431 reference voltage), the base drive to the TIP31 is reduced and the output current is limited to 1.5 A.

$$R1 = \frac{V_1 - (V_{be} + V_{RCL})}{I_1}$$

$$= \frac{12 - (1.8 + 2.5)}{0.06} = 128\ \Omega$$

$$R_{CL} = \frac{V_{ref}}{I_L} = \frac{2.5\ V}{1.5\ A} = 1.7\ \Omega$$

d) Voltmeter Scaler

The circuit in Figure 5–56 is a voltmeter scaler (or multiplier) to extend the range of a 0 to 10 V voltmeter to 40 V. Most multiplier circuits extend the range with 0 V being the low reading on any given scale. This circuit actually divides the 40 V total range into 4 separate 10 V scales.
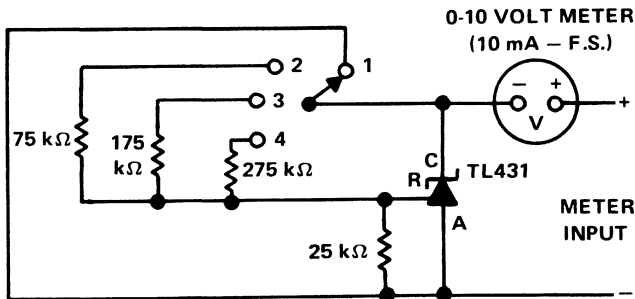
SWITCH POSITION	1	2	3	4
METER RANGE VOLTS	0-10	10-20	20-30	30-40

Fig. 5–56   Voltmeter Scaler

With the selector switch in position #1, the reference input of the TL431 is bypassed and the TL431 does not influence circuit operation. The meter is effectively connected directly to the voltage being measured. This scale would be the normal meter range of 0 to 10 V.

When in position #2, a 75 kΩ and a 25 kΩ resistor are added in series across the anode and cathode of the TL431. The voltmeter will remain near zero until the input reaches 10 V. At this time, there is 2.5 V between the reference terminal and anode which causes the voltmeter to start reading at 10 V. It will continue reading on this scale until it reaches full scale, which is 20 V.

This sequence is repeated in 10 V steps until position #4 is reached. This circuit is very useful when expanded-scale voltmeter multiplication is required. The precision of the scaler depends upon the accuracy of the resistors.

e) Voltage-Regulated, Current-Limited Battery Charger for Lead-Acid Batteries

There are a number of approaches to recharging lead-acid batteries. Many will return the battery to service, but fail to fully rejuvenate the battery. To keep a battery fully charged, and attain maximum battery life, proper charging techniques must be observed.

The status of a cell is determined by the specific gravity of the electrolyte solution. A specific gravity of 1.280 (obtained by hydrometer reading) indicates a fully charged cell. A reading of 1.250 or better is considered good. A fully discharged cell exhibits a specific gravity of 1.150 or less.

Battery Charger Design

The battery charger design shown in Figure 5–57 is based on a charging voltage of 2.4 V per cell, in accordance with most manufacturer's recommendations. The battery charger circuit pulses the battery under charge with 14.4 V (6 cells × 2.4 V per cell) at a rate of twice the supply voltage frequency.

The design provides current limiting to protect the charger's internal components while limiting the charging rate to prevent

damaging discharged lead-acid batteries. The maximum recommended charging current is normally about one-fourth the ampere-hour rating of the battery. For example, the maximum charging current for an average 44 ampere-hour battery is 11 A.

If the impedance of the load requires a charging current greater than the 11 A current limit, the circuit will go into current limiting. The amplitude of the charging pulses is controlled to maintain a maximum peak charging current of 11 A (8 A average).

The charger circuit is composed of four basic sections:

1. Rectifier

2. Voltage Regulator

3. Current Limiting

4. Series Pass Element
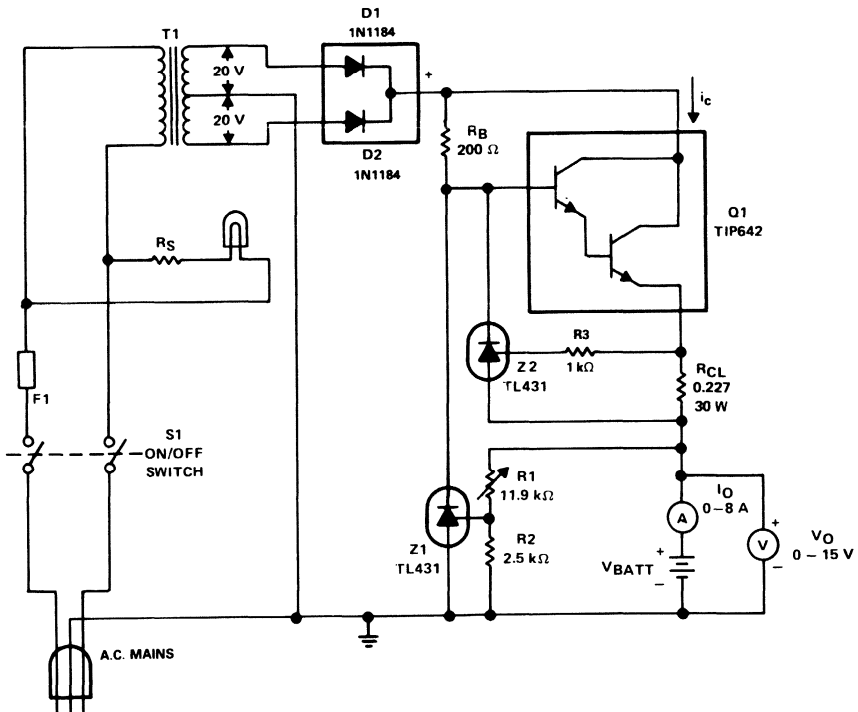
Fig. 5–57   Current Limited and Voltage Regulated Battery Charger.

Rectifier Section

A full-wave rectifier configuration with a centre-tapped transformer (Figure 5–58) achieves maximum performance with minimum component count. The breakdown voltage requirement for the diode is:

$$VR > 2 \times Vsecondary(pk) - V_F(rectifier\ drop)$$

$$\therefore VR > (40 \times 1.414) - 1 = 56\ V$$
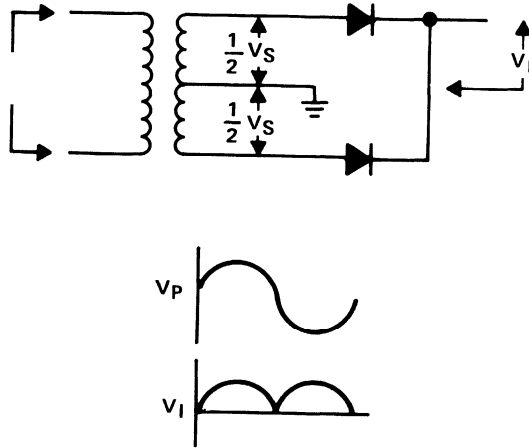
Fig. 5–58   Full-Wave Rectifier Section of Circuit.

This design is set to current limit at 11 A so a rectifier rating of 25 A is recommended to handle the maximum current drain plus any current surges. A pair of 1N1184 diodes was chosen (35 A/100 V rectifiers).

Voltage Regulator Section

The components which make up the voltage regulator portion of the circuit are: Z1, Q1, R1, R2 and R_B as shown in Figure 5–59.
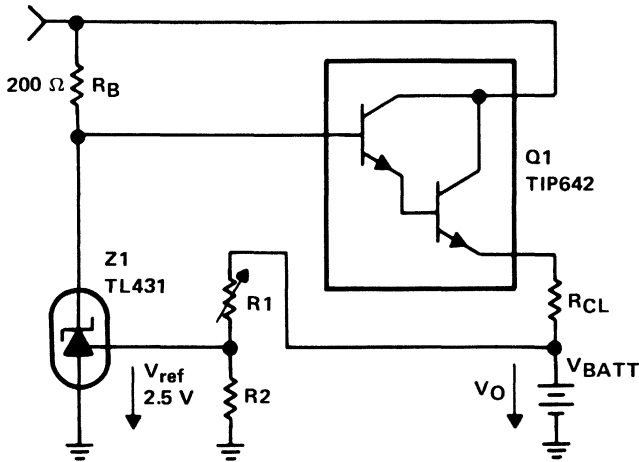
Fig. 5–59   Voltage Regulator Section of Circuit.

Z1 is a TL431 programmable shunt regulator which serves as the control element. Q1 is the pass transistor, and R1–R2 sense the output voltage providing feedback to Z1. R1 and R2 are chosen so that their node voltage is 2.5 V at the desired output voltage. This node voltage is applied to the TL431's error amplifier which compares it to the internal 2.5 V reference.

When the feedback voltage is less than the internal 2.5 V reference, the series impedance (anode-to-cathode) of the TL431 increases, decreasing the shunt current through the TL431. This increases the current available to the base of pass transistor Q1, increasing the output voltage.

When the feedback voltage is greater than the internal 2.5 V reference, the series impedance of the TL431 decreases, increasing the shunt current through the TL431. This decreases the current available to the base of Q1, decreasing the output voltage.

Because the feedback voltage is sensed at the output, the TL431 will compensate for any changes in the base-emitter drop of Q1 or the voltage dropped across R_{CL} for various currents.

Current Limiter Section

The components which make up the current-limit portion of this circuit are: Z2, Q1, ad R_{CL} as shown in Figure 5–60.
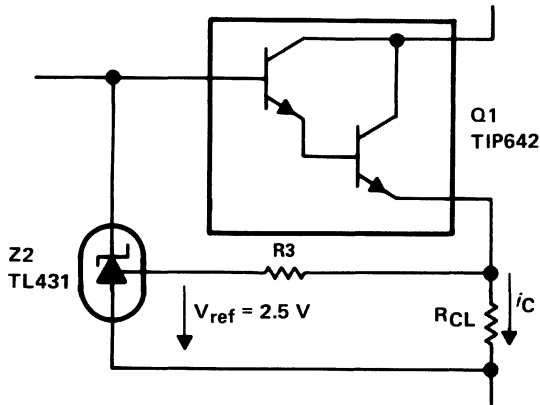
Fig. 5–60   Current Limiter Section of Circuit.

The value of the current-limit setting resistor, R_{CL}, is chosen so that 2.5 V will be developed across it at the desired limit current. The voltage across R_{CL} is sensed by a TL431 programmable shunt regulator (Z2). When the output current is less than the current limit, V_{ref} is less than 2.5 V and Z2 is a high impedance which does not affect the operation of Q1.

When the output current reaches maximum, V_{ref} is 2.5 V and the impedance of Z2 decreases, decreasing the current available at the base of Q1 and controlling the maximum output current. Under this condition, shunt regulator Z2 takes control of pass transistor Q1 and maintains a constant current, even into a short circuit. R3 is included to protect Z2 in the event that R_{CL} becomes open circuit.

Series Pass Element

The series pass element used in this configuration is a conventional Darlington power transistor, whose control is derived from either Z1 or Z2 depending on the state of the battery being charged. See Figure 5–61.
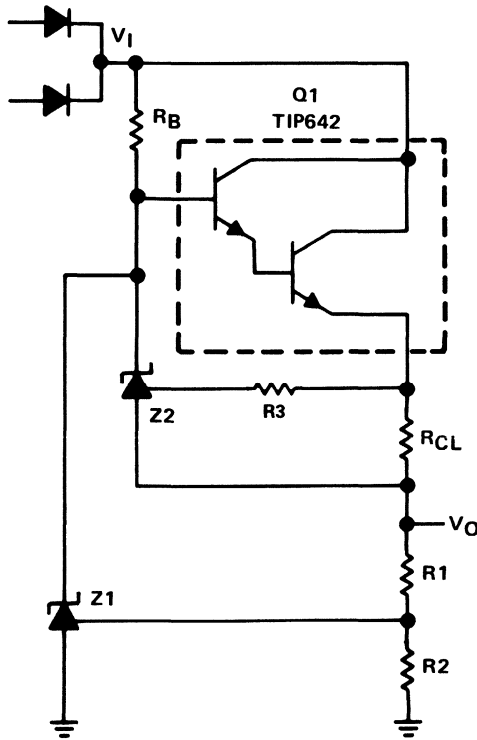
Fig. 5–61   Series Pass Element.

The performance characteristics of Q1 are important in determining the circuit design and in the choice of the transformer to be used. This relationship is shown in the following section on the design of the battery charger.

Design Calculations

The values of R1 and R2 set the output voltage level at 2.4 V per cell or 14.4 V for 6 cells. For optimum performance of Z1, 1 mA should flow through the R1 and R2 combination.

$$R1 + R2 = \frac{14.4\,V}{1\,mA} = 14.4\,k\Omega$$

$$R2 = \frac{2.5\,V}{1\,mA} = 2.5\,k\Omega$$

$$R1 = 14.4\,k\Omega - 2.5\,k\Omega = 11.9\,k\Omega$$

For ease of final adjustment, a 20 kΩ potentiometer may be used for R1.

Current limiting starts when 2.5 V is developed across R_{CL} at the desired current limit. For a 44 A hour battery, the maximum charge rate is 11 A.

$$R_{CL} = \frac{2.5\,V}{11\,A} = 0.227\,\Omega$$

After the pass transistor has been selected, its base drive resistor, R_B, may be calculated. A TIP642 meets the requirements. From the data sheet:

$$h_{FE} \text{ @ } 11\,A = 500\,(min)$$

$$V_{CE} \approx 2\,V$$

$$V_{BE} = 1.6\,V$$

$$P_{max} = 160\,W \text{ @ } 40°C\,TC$$

$$I_B = 22\,mA \text{ @ } 11\,A \text{ peak collector current}$$

To calculate R_B, assume a worst case or short-circuit condition where:

$$R_B \approx \frac{V_1 - V_{ref} - V_{BE(Q1)}}{I_B(Q1) + I_{SHUNT}(Z_2)}$$

$$R_B \approx \frac{27.28 - 2.5 - 1.6}{0.022 + 0.12} = 163\,\Omega$$

While R_B must be small enough so it does not limit the base current of Q1 at the desired I_{CHG} of 8 A, however, it must be large enough to limit the current during short circuit conditions. This value should be less than the sum of the base drive current required by Q1 and $I_{SHUNT(max)}$ Z2.

$$R_B \approx \frac{(V_1 - 14.4 \text{ V} - 2.5 \text{ V} - V_{BE}(Q1))}{I_{CHG}/h_{FE}(Q1)}$$

$$= \frac{27.28 - 14.4 - 2.5 - 1.6}{8/500}$$

$$R_B \approx \frac{8.78}{0.016} = 548.7 \; \Omega$$

A value of R_B within this range assures sufficient drive to Q1 for a charging rate of 8 A, yet allows total control of Q1 by Z2 during short-circuit conditions. R_B was selected to be 200 Ω.

uA723 PRECISION VOLTAGE REGULATOR

The uA723 monolithic integrated circuit voltage regulator is used extensively in power supply designs. The device consists of a temperature compensated reference amplifier, an error amplifier, a 150 mA series-pass transistor, and current-limiting circuitry. See Figures 5–62 and 5–63 for the functional diagram and schematic.

Additional external npn or pnp pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition, the device features low standby current drain, low temperature drift and high ripple rejection. The uA723 may be used with positive or negative supplies as a series, shunt, or floating regulator.

When using an external series pass device, the gain of the uA723 error amplifier must also be taken into consideration. Adequate uA723 compensation may be provided by connecting a 100 to 500 pF capacitor from the compensation terminal to the inverting input.

N.B. Extra capacitance may be required at both the input and output of any power supply due to the inductive effects of long lines. Adding output capacitance provides the additional benefit of reducing the output impedance at high frequencies.
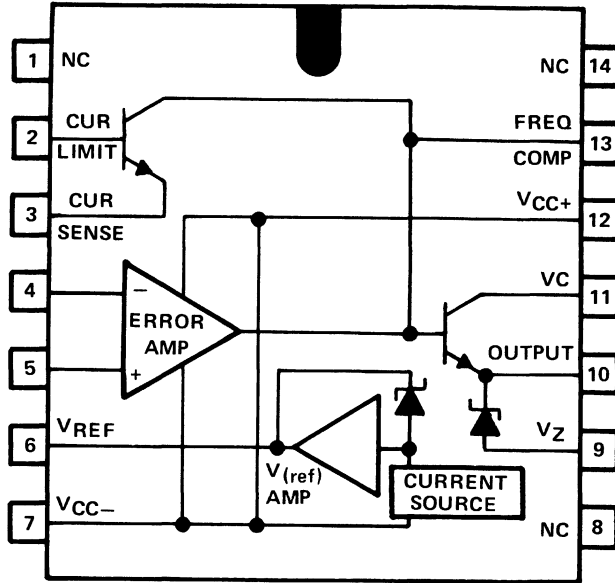
Fig. 5–62   uA723 Functional Block Diagram.
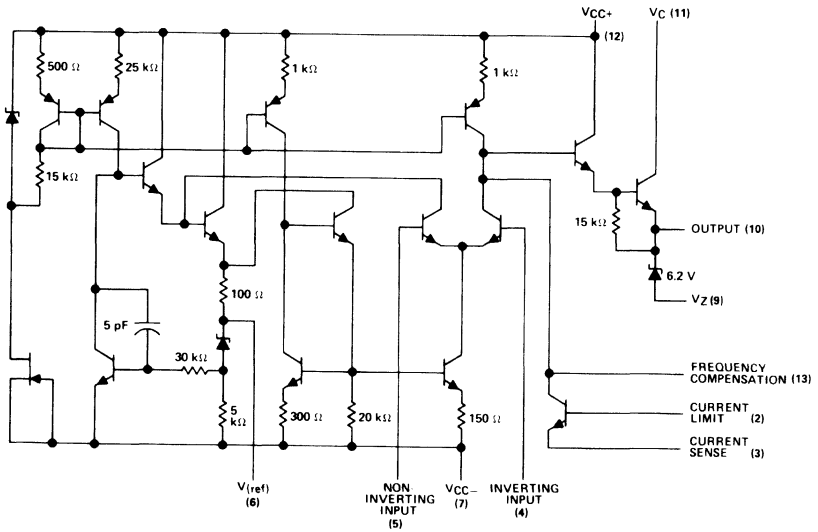
Fig. 5–63   uA 723 Schematic.

Typical Applications

The required output voltage and current limits for the applications shown in Figure 5–64 can be calculated from the equations given in Table 5–1. In all cases the resulting resistor values are assumed to include a potentiometer as part of the total resistance. Table 5–2 affords a quick reference for many standard output voltage requirements.

Table 5–1   Formulae for Output Voltages.

Outputs from +2 to +7 V
[Figures 5–64(a), (e), (f)]

$$V_O = V_{(ref)} \times \frac{R2}{R1 + R2}$$

Outputs from + 7 to +37 V
[Figures 5–64(b), (d), (e), (f)]

$$V_O = V_{(ref)} \times \frac{R1 + R2}{R2}$$

Outputs from −6 to −250 V
[Figure 5–64(c)]

$$V_O = - \frac{V_{(ref)}}{2} \times \frac{R1 + R2}{R1}$$

R3 = R4

Current Limiting $I_{(limit)} \approx \dfrac{0.65 \text{ V}}{R_{SC}}$

Foldback Current Limiting
[Figure 5–64(f)]

$$I_{(knee)} \approx \frac{V_O R3 + (R3 + R4)\, 0.65 \text{ V}}{R_{SC}\, R4}$$

$$I_{OS} \approx \frac{0.65 \text{ V}}{R_{SC}} \times \frac{R3 + R4}{R4}$$
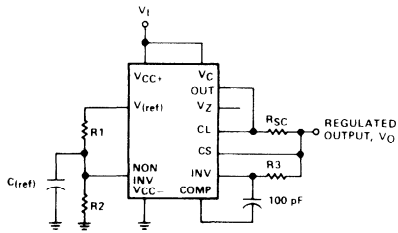
NOTES: A. $R3 = \dfrac{R1 \cdot R2}{R1 + R2}$ for minimum α_{VO}.

B.   R3 may be eliminated for minimum component count. Use direct connection (i.e., $R3 = 0$).

(a) BASIC LOW-VOLTAGE REGULATOR
($V_O = 2$ to 7 Volts)
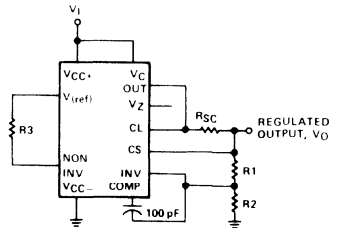
NOTES: A. $R3 = \dfrac{R1 \cdot R2}{R1 + R2}$ for minimum α_{VO}.

B.   R3 may be eliminated for minimum component count. Use direct connection (i.e., $R3 = 0$).

(b) BASIC HIGH-VOLTAGE REGULATOR
($V_O = 7$ to 37 VOLTS)
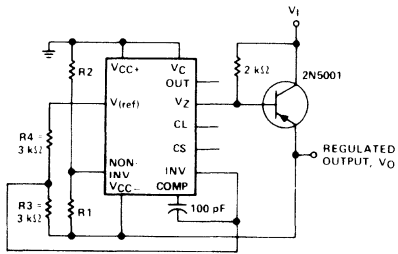
(c) NEGATIVE-VOLTAGE REGULATOR
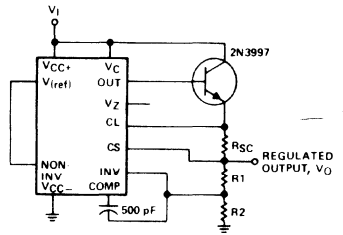
(d) POSITIVE-VOLTAGE REGULATOR
(EXTERNAL N-P-N PASS TRANSISTOR)
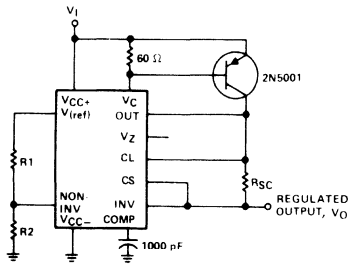
(e) POSITIVE-VOLTAGE REGULATOR
(EXTERNAL P-N-P PASS TRANSISTOR)
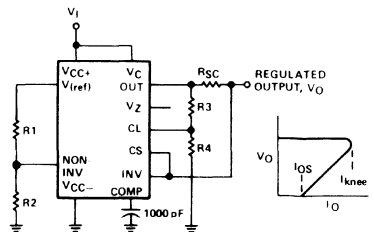
(f) FOLDBACK CURRENT LIMITING

Fig. 5–64   Typical Applications.

Table 5–2   Resistor Values for Standard Output Voltages.

OUTPUT VOLTAGE (V)	APPLICABLE FIGURE (5-64) SEE NOTE 1	FIXED OUTPUT ± 5% kΩ		ADJUSTABLE OUTPUT ± 10% kΩ		
		R1	R2	R1	P1	R2
+ 5.0	a, e, f	2.15	4.99	0.75	0.5	2.2
+ 6.0	a, e, f	1.15	6.04	0.5	0.5	2.7
+ 9.0	b, d, e, f	1.87	7.15	0.75	1.0	2.7
+ 12.0	b, d, e, f	4.87	7.15	2.0	1.0	3.0
+ 15.0	b, d, e, f	7.87	7.15	3.3	1.0	3.0
− 9.0	c see	3.48	5.36	1.2	0.5	2.0
− 12.0	c note 2	3.57	8.45	1.2	0.5	3.3
− 15.0	c	3.57	11.5	1.2	0.5	4.3

NOTES: 1. To make the voltage adjustable, the R1/R2 divider shown in the figures must be replaced by the divider shown here.
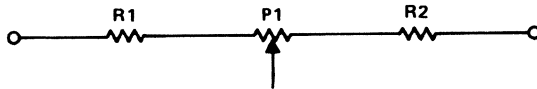
2. For negative output voltages less than 9 V, $V_{CC}+$ and V_C must be connected to a level large enough to allow the voltage between $V_{CC}+$ and $V_{CC}-$ to be greater than 9 V.

General Purpose Power Supply

The general purpose power supply shown in Figure 5–65 may be used for supply output voltages from 1 to 35 V.
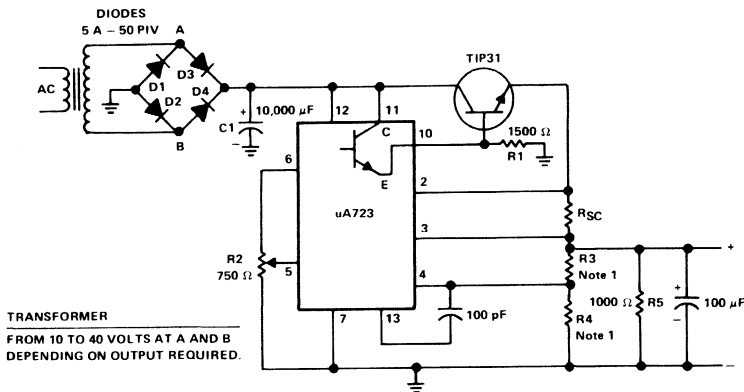
NOTE 1: FOR 14 V TO 35 V OUTPUT – R3 = 2 k, R4 = 500 Ω
FOR   1 V TO 14 V OUTPUT – R3 = 2 k, P4 = 2 k

CURRENT LIMIT $R_{SC} = \dfrac{0.65 \text{ V}}{I_{(limit)}}$

Fig. 5–65   General Purpose Power Supply.

The line transformer should be selected to give about 1.4 times the desired output voltage from the positive side of the filter capacitor, C1, to ground. R1 discharges the carriers in the base-emitter junction of the TIP31 when the drive is reduced. Its value is determined as follows:

$$R1 = \frac{\text{TIP31 Base Voltage (at point of conduction)}}{\text{Leakage Current of TIP31 and uA723 Output}}$$

where: TIP31 voltage at point of conduction is 0.35 V, leakage current (collector-base) of the TIP31 plus the collector-emitter leakage of the uA723 output transistor (worst case = 200 μA).

therefore: $R1 = \dfrac{0.35 \text{ V}}{0.0002 \text{ A}} = 1750 \ \Omega$ maximum

$R1 = 1.5 \ \Omega$ (standard value)

Potentiometer R2 sets the output voltage to the desired value by adjusting the reference input voltage. It is connected between pin 6 (7.15 V reference) and ground. The centre arm of R2, connected to pin 5, will select any point between zero and the 7.15 V reference.

Resistors R3 and R4 are connected in series across the supply output. The junction of these two resistors is connected to the inverting input (pin 4) of the error amplifier establishing an output voltage reference. This voltage reference is compared to the selected voltage at the non-inverting input to the error amplifier (pin 5) to set the level of output voltage regulation. The values for R3 and R4 are listed in Note 1 of Figure 5–65.

R_{SC} is the current limit set resistor. Its value is calculated as:

$$R_{SC} = \frac{0.65 \text{ V}}{I_L}$$

For example, if the maximum current output is to be 1 A, $R_{SC} = 0.65/1.0 = 0.65 \ \Omega$.

The 1 kΩ resistor, R_5, on the output is a light-load resistor designed to improve the no-load stability of the supply. The 100 μF electrolytic capacitor improves the overall output ripple voltage. A 100 pF capacitor from the compensation terminal (pin 13) to the inverting input (pin 4)

allows for gain variations in the uA723 error amplifiers and for parasitic capacitances.

The output voltage and current of this supply must be restricted to the specifications of the TIP31 series pass transistor. Since it is rated at two watts in free air at 25°C, sufficient heat sinking is necessary.

8-Amp Regulated Power Supply for Operating Mobile Equipment

It is often necessary to operate or test equipment used in automotive applications. This supply, as shown in Figure 5–66, provides up to 8 A at 13.8 V.
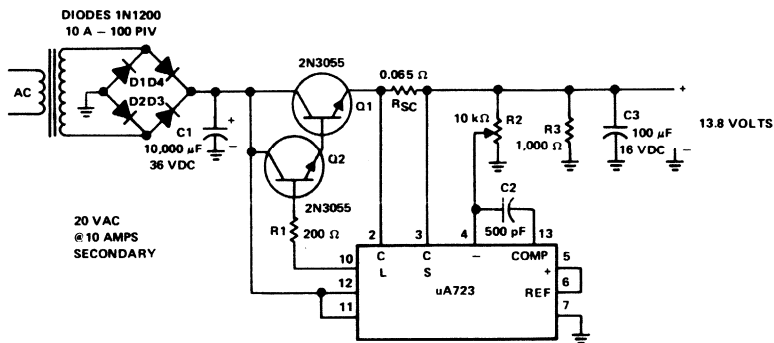
Fig. 5–66   8-Amp Regulated Power Supply.

The uA723 is used as the control element, furnishing drive current to series-pass transistors which are connected in a Darlington configuration. Two 2N3055 npn transistors are used as the pass transistors, so proper heat sinking is necessary to dissipate the power.

This supply is powered by a transformer operating from ac mains on the primary and providing approximately 20 V ac on the secondary. Four 10 A diodes with a 100 PIV rating are used in a full-wave bridge rectifier. A 10,000 μF/36 V dc capacitor completes the filtering, providing 28 V dc.

The dc voltage is fed to the collectors of Darlington-connected 2N3055's. Base drive for the pass transistors is from pin 10 of the uA723 through a 200 Ω current limiting resistor, R1. The reference terminal (pin 6) is tied directly to the non-inverting input of the error amplifier (pin 5), providing 7.15 V for comparison.

The inverting input to the error amplifier (pin 4) is fed from the centre arm of a 10 kΩ potentiometer connected across the output of the supply. This control is set for the desired output voltage of 13.8 V. Compensation of the error amplifier is accomplished with a 500 pF capacitor connected from pin 13 to pin 4.

The 1 kΩ resistor on the output is a light load to provide stability when the supply has a no load condition. The 100 μF/16 V dc electrolytic capacitor completes the filter action and reduces the ripple voltage.

The current output of the supply is sampled through resistor R_{SC} between the output transistor and the output terminal. The resistor value for a 10 A maximum current is calculated from the formula:

$$R_{SC} = \frac{0.65 \text{ V}}{I_{(load\ max)}} = \frac{0.65}{10} = 0.065 \ \Omega$$

If the power supply should exceed 8 A or develop a short circuit, the uA723 regulator will bias the transistors to cutoff and the output voltage will drop to near zero until the short circuit condition is corrected. This circuit features a no-load-to-full-load (8 A) voltage regulation of no more than 0.2 V dc variation (better than 2% regulation).

±15 Volts @ 1.0 Amp Regulated Power Supplies

When working with operational amplifiers, a common requirement is plus and minus supplies in the 15 V range. A positive 15 V supply is shown in Figure 5–67 and a negative 15 V supply is shown in Figure 5–68.
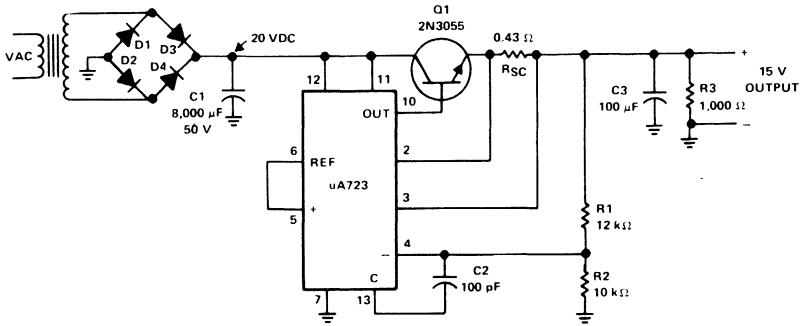
Fig. 5–67 +15-Volts at 1.0-Amp Regulated Power Supply.

Positive Supply

The positive supply, shown in Figure 5–67, receives +20 V dc from the rectifier/filter section. This is applied to pins 11 and 12 of the uA723 as well as to the collector of the 2N3055 series-pass transistor. The output voltage is sampled through R1 and R2 providing about 7 V with respect to ground at pin 4.

The reference terminal (pin 6) is tied directly to pin 5, the non-inverting input of the error amplifier. For fine trimming of the output voltage, a potentiometer may be installed between R1 and R2. A 100 pF capacitor from pin 13 to pin 4 furnishes gain compensation for the amplifier.

Base drive to the 2N3055 pass transistor is furnished by pin 10 of the uA723. Since the desired output of the supply is 1 A, maximum current limit is set to 1.5 A by resistor R_{SC} whose value is calculated as:

$$R_{SC} = \frac{0.65 \text{ V}}{I_{(max\ limit)}} = \frac{0.65}{1.5} = 0.433\ \Omega$$

A 100 μF electrolytic capacitor is used for ripple voltage reduction at the output. A 1 kΩ output resistor provides stability for the power supply under no-load conditions. The 2N3055 pass transistor must be mounted on an adequate heat sink since the 3.5 W, 25°C rating of the device would be exceeded at 1 A load current.

Negative Supply

The negative 15 V version of this power supply is shown in Figure 5–68.
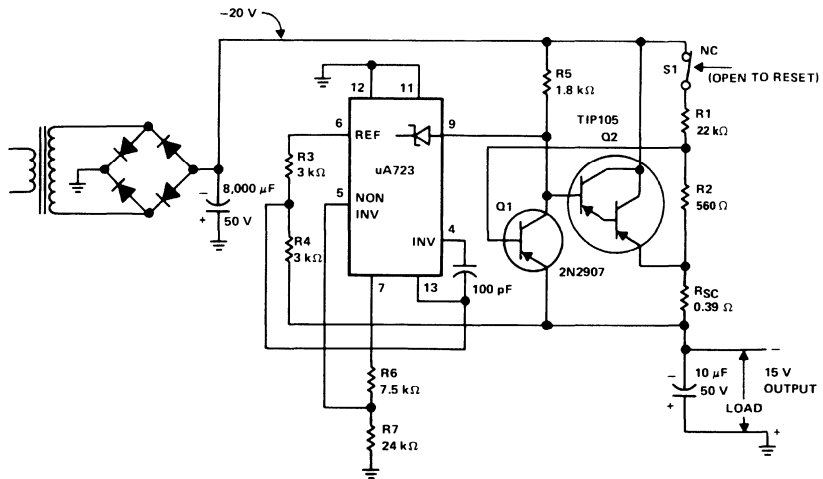
Fig. 5–68   15-Volts at 1.0 Amp Regulated Power Supply.

The supply receives −20 V from the rectifier/filter which is fed to the collector of the Darlington pnp pass transistor, a TIP105. A different uA723 configuration is required when designing a negative regulator.

The base drive to the TIP105 is supplied through resistor R5. The base of the TIP105 is driven from pin 9 (V_Z terminal), which is the anode of a 6.2 V zener diode that connects to the emitter of the uA723 output control transistor.

The method for providing the positive feedback required for foldback action is shown in Figure 5–68. This technique introduces positive feedback by increased current flow through resistors R1 and R2 under short-circuit conditions. This forward biases the base-emitter junction of the 2N2907 sensing transistor, which reduces base drive to the TIP105.

The final percentage of foldback depends on the relative contributions of the voltage drop across R2 and R_{SC} to the base current of the 2N2907 sensing transistor. From the start of base-emitter conduction of

the sense transistor to the full shut-off of the TIP105 pass transistor requires a 2 μA base current.

The latch condition, or 100% positive feedback, is generated by any change in the input voltage which increases the voltage drop across R2 turning on the sense transistor (2N2907). It can only be reset by breaking the positive feedback path with switch S1. This allows the series pass device to once more be driven in a normal fashion.

R3 and R4 are equal in value and divide the 7.15 V reference in half. The resulting 3.6 V reference is tied to the inverting input of the error amplifier. R6 and R7 are connected in series across the output of the power supply. The junction of R6 and R7 furnishes 3.6 V to the non-inverting input of the error amplifier. At this point the output is regulated at -15 V with respect to ground.

Resistors R1 and R2 are calculated as follows:

$$V_{R1} = (20 - 15.5)V$$

$$= 4.5V$$

Choose $R_1 = 22\,k\Omega$

$$\therefore I_{R1} = 0.2mA$$

$$R_2 = \frac{15.5 - 15.39}{0.2} = 550\Omega$$

$$= 560\Omega \text{ (standard value)}$$

Resistor $R5 = (V_I - V_O - V_{BEQ2} - VR_{SC})$

$$\times \frac{(\text{min beta Q2})}{I_M \,(\text{max load current})}$$

$$R5 = (20 - 15 - 2.8 - 0.4) \times \frac{1000}{1} = 1800\,\Omega$$

$$R5 = 1.8\,k\Omega$$

---

*V_{SENSE} is defined as the base to emitter voltage needed to start turn-on of the 2N2907. From the data sheet this is about 0.5 V.

The current sense resistor R_{SC} is calculated as follows:

$$R_{SC} = \frac{V_O}{I_M} \left(\frac{V_{SENSE}}{V_I - V_{SENSE}} \right) = \frac{15}{1} \left(\frac{0.5}{20 - 0.5} \right) = 0.384 \ \Omega$$

$$R_{SC} = 0.39 \ \Omega$$

Foldback limiting, as used in this circuit, is advantageous where excessive pass transistor power dissipation is a problem. The TIP105 can tolerate only 2 W dissipation in free air at 25°C ambient, so adequate heat sinking is necessary.

LOW DROP OUT VOLTAGE REGULATORS

A series pass regulator can maintain output regulation with much lower differential input-to-output voltage by using pnp instead of an npn transistor in the control element. The differential voltage at which regulation ceases is known as the 'drop out voltage'. Standard regulators have drop out voltages of 2 to 3 V; using a pnp transistor a low drop out regulator reduces this to 0.6 V.

Unfortunately improvements such as this are rarely without side effects. Low drop out regulators cost a little more than their standard counter parts because pnp transistors require more silicon area than npn. Also the pnp drive topology and lower gain of pnp transistors means the common pin bias current is significantly higher. The bias current also varies with output current.

Low drop out regulators are widely used in automotive applications to ensure a regulated output during 'cold cranking' conditions. Supporting this use these regulators normally also have transient voltage protection for load dump up to 60 V and protection against reverse battery connection or two battery jumps.

In other battery applications low drop out regulators allow a longer discharge (e.g. down to 5.6 V) before the output drops out of regulation. In some portable instruments it is possible to have a more effective cell arrangement that takes advantage of the wider operating range.

Power savings can be achieved in non battery applications if the input voltage is reduced to take advantage of the lower drop out voltage. However the higher bias current reduces the efficiency improvement to typically 10 to 20%.

As with standard devices, low drop out regulators require input and output bypass capacitors for proper regulator function. Typical values are 0.1 μF for the input and 10 to 100 μF for the output (depending on the device type).

VOLTAGE REGULATOR TERMS AND DEFINITIONS

Series Regulators

Input Regulation

The change in output voltage, often expressed as a percentage of output voltage, for a change in input voltage from one level to another.

NOTE: Sometimes this characteristic is normalized with respect to the input voltage change.

Ripple Rejection

The ratio of the peak-to-peak input ripple voltage, to the peak-to-peak output ripple voltage.

NOTE: This is the reciprocal of ripple sensitivity.

Ripple Sensitivity

The ratio of the peak-to-peak output ripple voltage, sometimes expressed as a percentage of output voltage, to the peak-to-peak input ripple voltage.

NOTE: This is the reciprocal of ripple rejection.

Output Regulation

The change in output voltage, often expressed as a percentage of output voltage, for a change in load current from one level to another.

Temperature Coefficient of Output Voltage (αV_O)

The ratio of the change in output voltage, usually expressed as a percentage of output voltage, to a change in temperature. This is the average value for the total temperature change.

$$\alpha V_O = \pm \left[\frac{(V_O \text{ at } T_2) - (V_O \text{ at } T_1)}{V_O \text{ at } 25°C} \right] \times \frac{100\%}{T_2 - T_1}$$

Output Voltage Change with Temperature

The percentage of change in the output voltage for a change in temperature. This is the net change over the total temperature range.

Output Voltage Long-Term Drift

The change in output voltage over a long period of time.

Output Noise Voltage

The rms output voltage, sometimes expressed as a percentage of the dc output voltage, with constant load and no input ripple.

Current-Limit Sense-Voltage

A voltage that is a function of the load current and is normally used for control of the current-limiting circuitry.

Dropout Voltage

The input-to-output differential voltage at which the circuit ceases to regulate against further reductions in voltage.

Feedback Sense Voltage

The voltage that is a function of the output voltage, used for control of the regulator.

Reference Voltage

The voltage that is compared with the feedback sense voltage to control the regulator.

Bias Current

The difference betwen input and output currents.

NOTE: This is sometimes referred to as quiescent current.

Standby Current

The input current drawn by the regulator with no output load and no reference voltage load.

Short-Circuit Output Current

The output current of the regulator with the output shorted.

Peak Output Current

The maximum output current that can be obtained from the regulator.

SHUNT REGULATORS

NOTE: These terms and symbols are based on JEDEC and IEC standards for voltage regulator diodes.

Shunt Regulator

A device having a voltage current characteristic similar to that of a voltage regulator diode. It is normally biased to operate in a region of low differential resistance (corresponding to the breakdown region of a regulator diode) and develops across its terminals an essentially constant voltage throughout a specified current range.

Anode

The electrode to which the regulator current flows within the regulator when it is biased for regulation.

Cathode

The electrode from which the regulator current flows within the regulator when it is biased for regulation.

Reference Input Voltage (V_{ref}) (of an adjustable shunt regulator)

The voltage at the reference input terminal with respect to the anode terminal.

Temperature Coefficient of Reference Voltage (V_{ref})

The ratio of the change in reference voltage to the change in temperature. This is the average value for the total temperature change. To obtain a value in ppm/°C:

$$V_{ref} = \left[\frac{(V_{ref} \text{ at } T_2) - (V_{ref} \text{ at } T_1)}{V_{ref} \text{ at } 25°C} \right] \left[\frac{10^6}{T_2 - T_1} \right]$$

Regulator Voltage (V_Z)

The dc voltage across the regulator when it is biased for regulation.

Regulator Current (I_Z)

The dc current through the regulator when it is biased for regulation.

Regulator Current near Lower Knee of Regulation Range (I_{ZK})

The regulator current near the lower limit of the region within which regulation occurs; this corresponds to the breakdown knee of a regulator diode.

Regulator Current at Maximum Limit of Regulation Range (I_{ZM})

The regulator current above which the differential resistance of the regulator significantly increases.

Differential Regulator Resistance (r_z)

The quotient of a change in voltage across the regulator and the corresponding change in current through the regulator when it is biased for regulation.

Noise Voltage (V_{nz})

The rms voltage across the regulator with the regulator biased for regulation and with no input ripple.

FIXED OUTPUT VOLTAGE REGULATORS

POSITIVE OUTPUT REGULATORS (SERIES)				
DEVICE SERIES	OUTPUT VOLTAGE TOLERANCE	MINIMUM DIFFERENTIAL VOLTAGE	OUTPUT CURRENT RATING	AVAILABLE VOLTAGE SELECTIONS
LM340	± 4%	2 V	1.5 A	3 : (5 V to 15 V)
TL780-00C	± 1%	2 V	1.5 A	3 : (5 V to 15 V)
uA7800C	± 4%	2 V to 3 V	1.5 A	9 : (5 V to 24 V)
uA78L00C	± 10%	2 V to 2.5 V	100 mA	8 : (2.6 V to 15 V)
uA78L00AC	± 5%	2 V	100 mA	8 : (2.6 V to 15 V)
uA78M00C	± 5%	2 V to 3 V	500 mA	8 : (5 V to 24 V)

NEGATIVE OUTPUT REGULATORS (SERIES)				
DEVICE SERIES	OUTPUT VOLTAGE TOLERANCE	MINIMUM DIFFERENTIAL VOLTAGE	OUTPUT CURRENT RATING	AVAILABLE VOLTAGE SELECTIONS
uA7900C	± 5%	2 V to 3 V	1.5 A	8.5 V to 24 V
MC79L00AC	± 5%	2 V	100 mA	3.5 V to 15 V
uA79M00C*	± 5%	2 V to 3 V	500 mA	7.5 V to 24 V

AVAILABLE OUTPUT VOLTAGES FOR ABOVE REGULATOR SERIES														
DEVICE SERIES	VOLTAGE SELECTIONS													
	2.6	5	5.2	6	8	8.5	9	10	12	15	18	20	22	24
LM340		X							X	X	X			
MC79L00AC		X							X	X				
TL780-00C		X							X	X				
uA7800C		X		X	X	X		X	X	X	X			X
uA78L00C	X	X		6.2	X		X	X	X	X				
uA78L00AC	X	X		6.2	X		X	X	X	X				
uA78M00C*		X		X	X			X	X	X		X		X
uA7900C		X	X	X	X				X	X	X			X
uA79M00C*		X		X	X				X	X		X		X

*Also available in Military Temperature Range (M suffix)

ADJUSTABLE OUTPUT VOLTAGE REGULATORS

POSITIVE OUTPUT SERIES REGULATORS				
DEVICE NUMBER	DIFFERENTIAL VOLTAGE MIN	MAX	OUTPUT VOLTAGE MAX	OUTPUT CURRENT RATING
LM317	1.2 V	37 V	$V_I - 1.2$ V	1.5 A
TL317	1.2 V	32 V	$V_I - 1.2$ V	100 mA
TL783	1.25 V	125 V	125 V	700 mA
uA723C*	3 V	38 V	37 V	25 mA

NEGATIVE OUTPUT SERIES REGULATORS				
DEVICE NUMBER	DIFFERENTIAL VOLTAGE MIN	MAX	OUTPUT VOLTAGE MAX	OUTPUT CURRENT RATING
LM337	1.2 V	37 V	$V_I + 1.2$ V	1.5 A

POSITIVE SHUNT REGULATORS					
DEVICE NUMBER	SHUNT VOLTAGE MIN	MAX	SHUNT CURRENT MIN	MAX	TEMP. COEFF. MAX
TL430C	3 V	30 V	2 mA	100 mA	200 ppm/°C
TL431C	2.55 V	36 V	1 mA	100 mA	100 ppm/°C
TL431I**	2.55 V	36 V	1 mA	100 mA	100 ppm/°C

*Also available in Military Temperature Range (M suffix)
**I denotes Industrial Temperature Range

LOW DROP OUT VOLTAGE REGULATORS

DEVICE SERIES	POSITIVE OUTPUT SERIES REGULATORS			
	OUTPUT VOLTAGE TOLERANCE	MINIMUM DIFFERENTIAL VOLTAGE	OUTPUT CURRENT RATING	AVAILABLE SELECTIONS
LM2930	±10%	0.6 V	150 mA	2 : (5 to 8 V)
LM2931	± 5%	0.6 V	150 mA	2 : (5 V)
TL750M00*	± 2%	0.7 V	750 mA	4 : (5 to 12 V)
TL751M00*	± 2%	0.7 V	750 mA	4 : (5 to 12 V)
TL750L00*	± 2%	0.7 V	100 mA	4 : (5 to 12 V)
TL751L00*	± 2%	0.7 V	100 mA	4 : (5 to 12 V)

*Future products

SWITCHING VOLTAGE REGULATORS

FEATURES	DEVICE NUMBER								
	SG3524	SG3525A	SG3527A	TL493	TL594	TL595	TL496C*	TL497A	MC34060
Fixed on Time							X	X	
Fixed Frequency PWM	X	X	X	X	X	X			X
General Purpose	X	X	X	X	X	X		X	X
Special Purpose							X		
On Chip Reference	X	X	X	X	X	X	X	X	X
On Chip Precision Reference		X	X	X	X	X			
Inhibit Control	X	X	X	X	X	X		X	
Dead Time ADJ.		X	X	X	X	X			X
On Chip Regulator						X			X
Current Sense Amp.				X			X	X	
Error Amp.	2	1	1	1	2	2			2
Expandable		X	X	X	X	X			
Double Pulse Prot.			X	X	X	X			
Operatable to 40V	35V	35V	35V	X	X	X			X
Operatable above 40V						X			
Internal soft start	X	X	X						
Under voltage Lockout		X	X		X	X			
Totem Pole output		X	X						
Parallelable outputs				X	X	X			
Single ended output							X	X	X
Double ended output	X	X	X	X	X	X			
Packages	D, J, N	J, N	J, N	J, N	D, J, N	J, N	PJG	J, N	J, N

*Only available in commercial (0–70°C) temp. range.

Section 6

Switching Power Supply Design

Modern electronic equipment usually requires one or more dc power sources. The two types of dc power supplies in common use are classified by the types of regulator employed; linear regulator or switching regulator.

Linear power supplies consist of a power transformer, rectifier and filter circuits, and a linear regulator. Direct-off-line switching power supplies don't require line transformers; the ac input is rectified and filtered, chopped by a high frequency transistor switch/transformer combination, then rectified and filtered again. Some switching supplies use a line transformer, the "chopping" being at a lower voltage, although the trend is towards direct-off-line designs. Switching techniques are also widely used to convert from an existing dc voltage to another for local auxiliary needs.

Switching power supplies have been used for some time in the military and space industry due to their smaller size and higher efficiency. In 1975 switching power supplies were more cost effective than linear power supplies from approximately the 500 W power level. Now the breakeven point can be as low as 5 W.

BASIC OPERATION OF SWITCHING REGULATORS

Figure 6–1 is a block diagram of a typical switching power supply which consists of four basic circuits:

1. Input rectifier and filter.

2. High frequency inverter.

3. Output rectifier and filter.

4. Control circuit.

The ac line voltage is applied to an input rectifier and filter circuit. The dc voltage output from the rectifer and filter circuit is switched at a higher frequency (typically 25 kHz to 100 kHz) by the transistor switch in the high frequency inverter circuit. This circuit contains either a high

50-60 Hz   **DC**   **20–100 kHz**   **DC**

**HIGH FREQUENCY
INVERTER**

LINE

OUTPUT

**INPUT RECTIFIER
AND FILTER**

**CONTROL
CIRCUIT**

**OUTPUT RECTIFIER
AND FILTER**

PWM

Osc   **Ref**
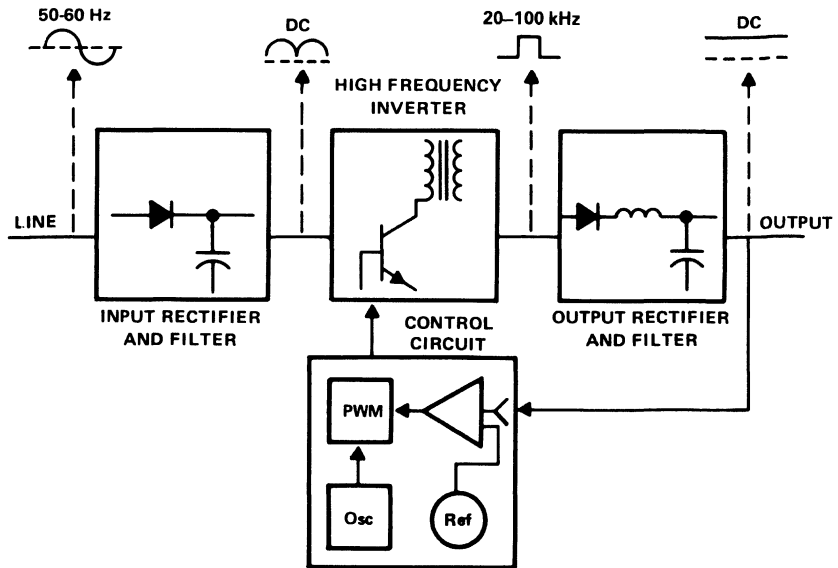
Fig. 6–1   Basic Direct-off-line Switching Regulator Block Diagram.

frequency transformer or inductor, depending on the output voltage required.

Output from the high frequency inverter circuit is applied to the output rectifier and filter circuit. The circuit is monitored and controlled by the control circuit which attempts to keep the output at a constant level.

The control circuit consists of an oscillator driving a pulse-width modulator, an error amplifier, and a precision voltage reference. The error amplifier compares the input reference voltage with a sample of the voltage from the output rectifier and filter circuit. As the load increases the output voltage drops. The error amplifier senses this drop and causes the pulse-width modulator to remain on for a longer period of time, delivering wider pulses to the transistor switch.

The width of the pulse determines how long the transistor switch allows current to flow through the high frequency transformer and, ultimately, how much voltage is available at the output. If the load decreases, narrower control pulses are delivered to the switching transistor causing the output voltage to remain at a constant value.

Advantages of a Switching Regulator

The primary advantages of switching regulators are higher efficiency and smaller size. Conventional linear series and shunt regulators operate in a continuous conduction mode, dissipating relatively large amounts of power. The efficiency of linear regulators is typically around 40% to 50%. When the input-to-output voltage differential is large, the resultant efficiency is much lower than 40%.

Switching regulators have typical efficiencies of 60% to 90%; much higher than either the linear series or shunt regulator. Switching regulators achieve their higher efficiency because the power-transistor switch is always turned completely on or off, except when it is switching between these states. The result is either low voltage or low current during most of its operation.

Switching regulators use the on-off duty cycle of the transistor switch to regulate the output voltage and current. By using a frequency much higher than the line frequency the transformers, chokes, capacitors and other filter elements can be made smaller, lighter, and less costly.

Disadvantages of a Switching Regulator

Switching regulators can generate some electromagnetic and radio frequency interference (EMI/RFI) noise due to high switching currents and short rise and fall times. EMI/RFI noise, which is generated at higher frequencies (100 kHz to 500 kHz), is easily filtered. In those applications where a large series impedance appears between the supply and the regulator, the rapid changes in current also generate a certain amount of noise.

These problems may be overcome or significantly reduced by one of the following steps:

1. Reducing the series impedance.

2. Increasing the switching time.

3. Filtering the input and output of the regulator.

Switching regulators with a fixed frequency are easier to filter than regulators with a variable frequency because the noise is at only one frequency and is periodic. Variable frequency regulators with a fixed 'on' time increase or decrease the switching frequency in proportion to load changes, presenting a more difficult filtering problem.

Basic Switching Regulator Architecture

There are three basic switching regulator configurations from which the majority of present day circuits are derived:

1. Step-down, or 'buck', regulator.

2. Step-up, or 'boost', regulator.

3. Inverting, or 'flyback' regulator (which is a variation of the 'boost' regulator).

The Step-down Regulator

Figure 6–2 illustrates the basic step-down or 'buck' regulator. The output voltage of this configuration is always less than the input voltage.
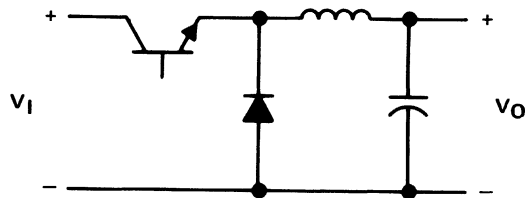
Fig. 6–2   Step-Down or 'Buck' Switching Regulator Circuit.

In the buck circuit, a semiconductor switch is placed in series with the dc input from the input rectifier/filter circuit. The switch interrupts the dc input voltage providing a variable-width pulse to a simple averaging LC filter. When the switch is closed, the dc input voltage is applied across the filter and current flows through the inductor to the load. When the switch is open, the energy stored in the field of the inductor maintains current through the load via the diode.

In the buck circuit, peak switching current is proportional to the load current. In the ideal case the output voltage is equal to the input voltage times the duty cycle.

$V_O = V_I \times$ Duty Cycle

The Step-Up Regulator

Another basic switching regulator configuration is the step-up or 'boost' regulator (Figure 6–3). In this type of circuit, the output voltage is always greater than the input voltage.
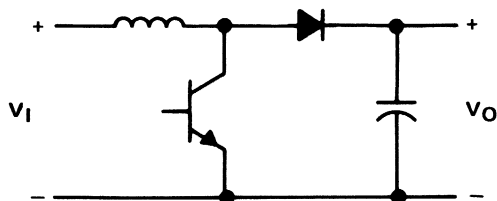
Fig. 6–3   Step-Up or 'Boost' Switching Regulator Circuit.

The boost circuit first stores energy in the inductor and then delivers this stored energy along with energy from the dc input voltage to the load. When the switch is closed, current flows through the inductor and the switch, charging the inductor but delivering no current to the load. When the switch is open, the voltage across the load equals the dc input voltage plus the voltage due to the energy stored in the inductor. The inductor discharges, delivering current to the load.

The peak switching current in the boost circuit is not related to the load current. The power output of a boost regulator can be determined by the following equation:

$$P_{OUT} = \frac{LI^2f}{2}$$

where:

P_{OUT} = power output

L = inductance

I = peak input current

f = operating frequency

The Inverting Regulator

The third switching regulator configuration is the inverting or 'flyback' regulator. This circuit is a variation of the step-up or 'boost' circuit discussed previously. The flyback circuit is illustrated in Figure 6–4.
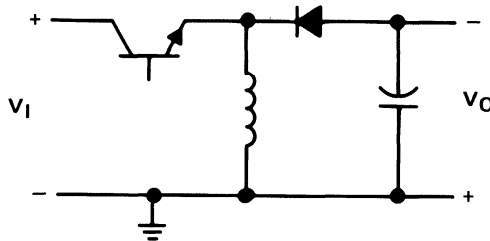
Fig. 6–4   Inverting or 'Flyback' Switching Regulator Circuit.

Flyback regulators, which evolved from 'boost' regulators, deliver only the energy stored by the inductor to the load. This type of circuit can step the input voltage up or down. When the switch is closed the inductor is charged, but no current is delivered to the load because the diode is reverse biased. When the switch is open the blocking diode is forward biased and the energy stored in the inductor is transferred through it to the load.

To determine the output voltage of an electronic equipment supply, the load (R_L) must be known. If the load is known, the output voltage may be calculated using the following equation:

$$V_O \sqrt{P_O R_L} = I \sqrt{\frac{L f R_L}{2}}$$

where:

V_O = voltage output

P_O = power out

R_L = load resistance

I = inductor current

f = operating frequency

The inductor current is proportional to the 'on time' (duty cycle) of the switch and regulation is achieved by varying the duty cycle.

Transient response to abrupt changes in the load is difficult to analyse. Practical solutions include limiting the minimum load and using the proper amount of filter capacitance to give the regulator time to respond to this change. Flyback type circuits are used at power levels of up to 100 W.

Forward Converters

The forward converter family, which includes the push-pull and half-bridge circuits, evolved from the step-down or 'buck' type of regulator. A typical forward converter circuit is illustrated in Figure 6–5.
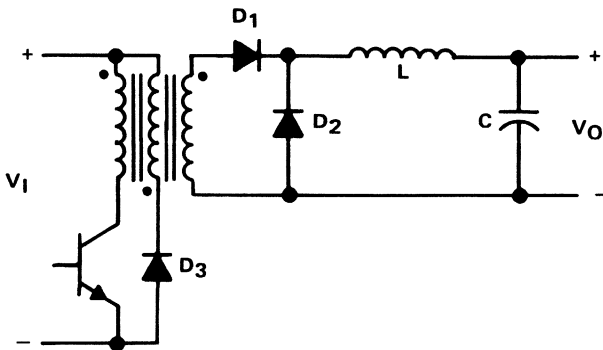
Fig. 6–5   Forward Converter Switching Regulator.

When the transistor switch is turned on the transformer delivers power to the load through diode D1 and the LC filter. When the switch is turned off diode D2 is forward biased and maintains current to the load.

Without the third winding, and diode D3, the converter would lose efficiency at higher frequencies. The function of this winding is to return energy stored in the transformer to the line and rest the transformer core after each cycle of operation.

This is a popular low power (up to about 200 W) converter and is almost immune to transformer saturation problems if conduction time is limited to less than half the period.

Push-Pull Converter

The push-pull converter is probably one of the oldest switching regulator type circuits. It was first used in the 1930's with mechanical vibrators functioning as the switch. When transistors became available push-pull converters were used as free-running oscillators in the primary of many automobile communication converters. Some recreational vehicles still use this free-running type of oscillator converter in dc-to-dc converters as well as in dc-to-ac inverters.

A typical push-pull converter circuit is shown in Figure 6–6.
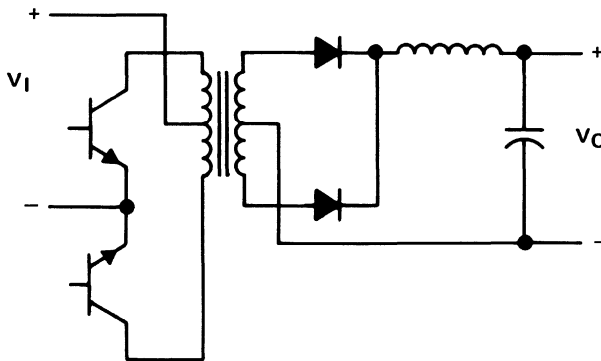
Fig. 6–6   Basic Push-Pull Converter Circuit.

Half Bridge Converter

The most popular type of high power converter is the half bridge circuit illustrated in Figure 6–7.

The half bridge converter has several advantages over the push-pull circuit: First, the midpoint between the capacitors (point A) is charged to $V_I/2$. This allows the use of transistors with lower breakdown voltage. Second, because the primary is driven in both directions (push-pull), a
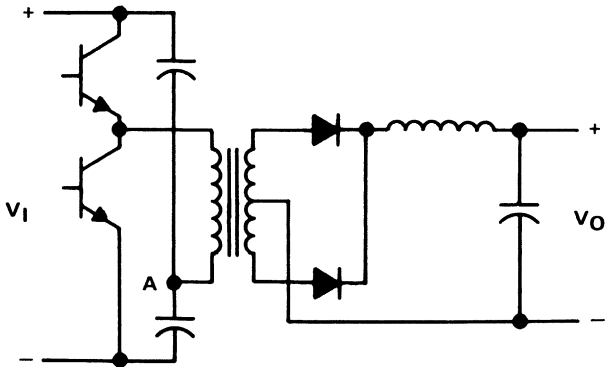
Fig. 6–7   Half Bridge Converter Circuit.

full-wave rectifier and filter are used which allows the transformer core to be more effectively utilized.

Full Bridge Converter

In contrast to the half bridge, the full bridge (or H-Bridge) converter uses four transistors as shown in Figure 6–8.
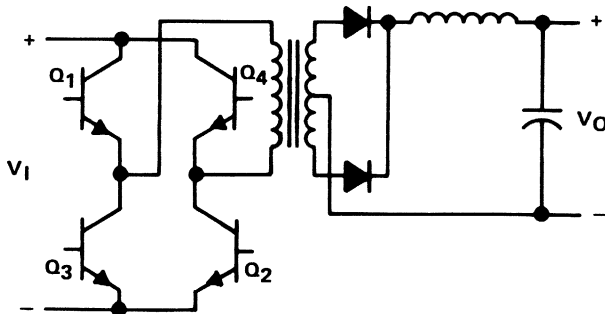
Fig. 6–8   Full Bridge Converter Circuit.

In a full bridge circuit the diagonally opposite transistors (Q1/Q2 or Q3/Q4) are turned on during alternate half cycles. The highest voltage any transistor is subjected to is V_I rather than $2 \times V_I$ as is the case in the push-pull converter circuit. The full bridge circuit offers increased reliability because less voltage and current stress is placed on the transistor than in previous configurations.

The disadvantage of this circuit is the space required by the four transistors, although offset by capacitor size savings, and the cost of the two additionl transistors.

THE TL594 CONTROL CIRCUIT

The TL594 is a fixed frequency pulse-width-modulation control for switching power supplies and voltage converters. The TL594 includes an adjustable oscillator, a pulse width modulator, and an error amplifier. Additional functions include over-current detection, independent dead-time control, a precision 5 V reference regulator, and output control logic which allows single-ended or push-pull operation of the two switching transistors. Figure 6–9 shows a block diagram of the TL594.
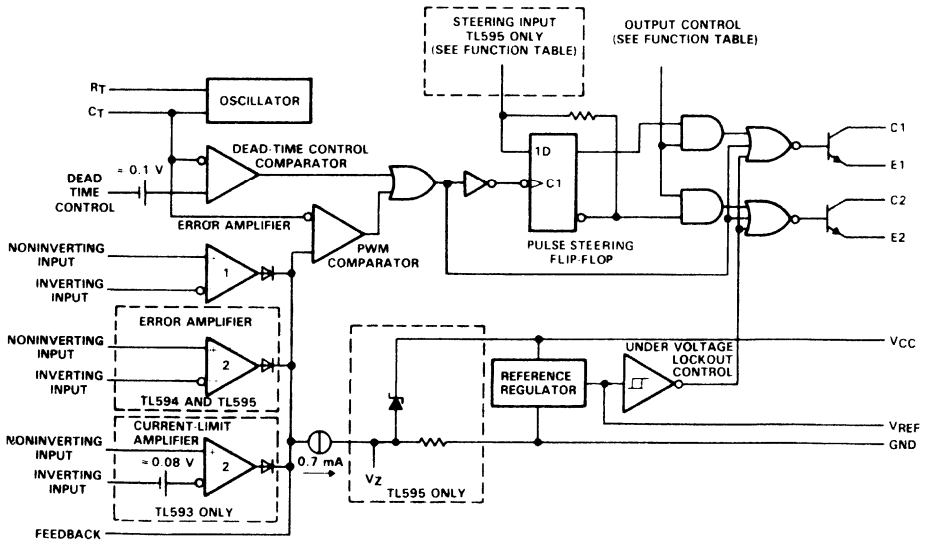
Fig. 6–9   TL594 Block Diagram.

Modulation of the output pulses is accomplished by comparing the sawtooth waveform created by the internal oscillator on timing capacitor C_T to either of two control signals. The output stage is enabled when the sawtooth voltage at pin 5 is greater than the voltage of the control signal. See Figure 6–10

PWM CONTROL RANGE, PIN 3

RESULTANT OUTPUT PULSE WITH
PIN 3 VOLTAGE AS ABOVE PIN 13 WIRED FOR
SINGLE ENDED OPERATION
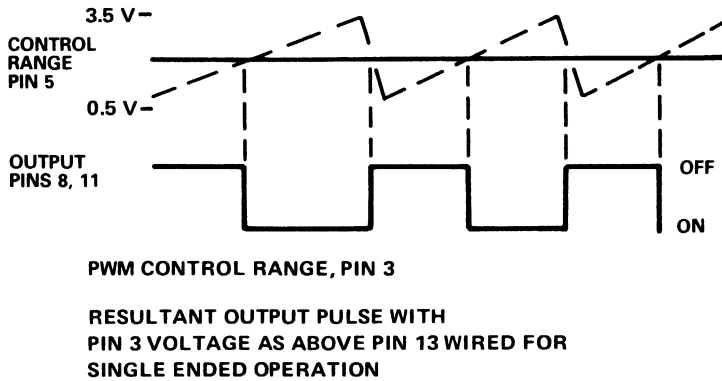
Fig. 6–10   Output Pulses vs. Sawtooth Control Voltage.

As the control signals increase the output pulse width decreases. The control signals are derived from two sources: the dead-time control and the error amplifiers. The dead-time comparator has a fixed offset of 100 mV which provides a preset dead time of about 5%. This is the minimum dead time that can be programmed with pin 4 grounded.

The pulse-width-modulation (PWM) comparator generates the control difference signal from the input created by either of the error amplifiers. One error amplifier is used to monitor the output voltage and provide a change in control signal voltage. The other error amplifier monitors the output current and its change in control voltage provides current limiting.

Reference Regulator

The internal 5-volt reference at pin 14 provides a stable reference for the control logic, pulse steering flip-flop, oscillator, dead-time control comparator and pulse-width-modulation circuitry. It is a band-gap circuit with short circuit protection and is internally programmed to an accuracy of ±1%.

Oscillator

The internal oscillator provides a positive sawtooth waveform to the dead-time and PWM comparators for comparison with the various

control signals. The oscillator frequency is set by an external timing capacitor and resistor on pins 5 and 6. The oscillator frequency is determined by the equation:

$$f_{OSC} = \frac{1}{R_T C_T} \text{ (single-ended applications)}$$

The oscillator frequency is equal to the output frequency only for single-ended applications. The output frequency for push-pull applications is one-half the oscillator frequency as shown by the equation:

$$f_{OSC} = \frac{1}{2\, R_T C_T} \text{(push-pull applications)}$$

There is a frequency variation of $\pm10\%$ between devices due to internal component tolerances.

The oscillator charges the external timing capacitor, C_T, with a constant current which is determined by the external timing resistor, R_T. This circuit produces a linear ramp voltage waveform. When the voltage across the timing capacitor reaches 3.5 V, the circuit discharges and the charging cycle is initiated again.

Dead Time and PWM Comparators

Both the dead time and PWM comparator functions use a single logic comparator with parallel input stages. The comparator output is a pulse-width-modulated signal, whose width is determined by comparison with the oscillator ramp waveform. The comparator outputs drive the output control logic.

A fixed internal 100 mV offset voltage to the dead-time comparator allows a minimum dead time between output pulses to be maintained when the dead-time control input (pin 4) is grounded (Figure 6–11).

The full range of pulse width control (0%–90%) is available when the dead time control voltage (pin 4) is between 3.0 V and 0 V. The relationship between control voltage and maximum output pulse width is essentially linear. A typical application for this may be in a push-pull converter circuit where overlap of the conduction times of power transistors must be avoided.

3.0 V—

0.2 V—

100 mV   DEADTIME OFFSET PIN 4 = 0 V

|←——— 90% ———→|

OSCILLATOR RAMP, PIN 5

MAXIMUM OUTPUT PULSE WIDTH
SINGLE ENDED OPERATION, PIN 4 = 0 V
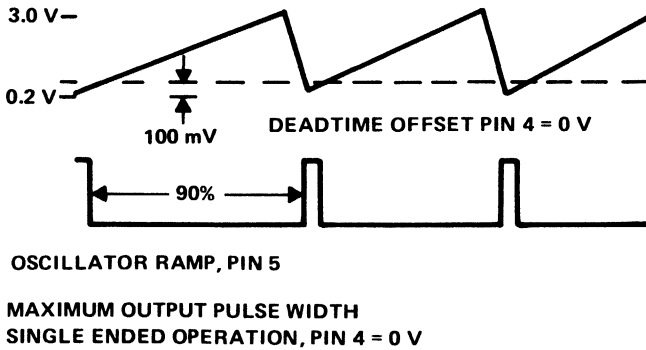
Fig. 6–11   Deadtime Comparator Operation.

The PWM comparator input is coupled internally to the outputs of the two error amplifiers. This input is accessible on pin 3 for control loop compensation. The output width from 90% of the period to zero as the voltage present at pin 3 varies from 0.5 V to 3.5 V (Figure 6–11).

Error Amplifiers

Both error amplifiers are high gain amplifiers which operate as single-ended single-supply amplifiers, in that each output is active high only. This allows each amplifier to pull up independently for a decreasing output pulse width demand. With the outputs ORed together, the amplifier with higher output level dominates. The minimum open loop gain of these amplifiers is 70 dB. Both error amplifiers exhibit a response time of about 400 ns from their inputs on pin 3. Figure 6–12 shows the Bode plot of the gain verses frequency.

80

60

40

GAIN (dB)

20

0
    1K   10K   100K   1M
      FREQUENCY (Hz)

AMPLIFIER BODE PLOT

Fig. 6–12   Amplifier Performance Curves.

Output Logic Control

The output control logic interfaces the pulse width modulator to the output stages. In the single-ended mode (both outputs conducting simultaneously) the pulse width modulated signal is gated through to both output stages when the output control (pin 13) is connected to ground.

For push-pull operation (each output stage conducting alternately) the output control (pin 13) is connected to the internal reference voltage (pin 14) enabling the pulse steering 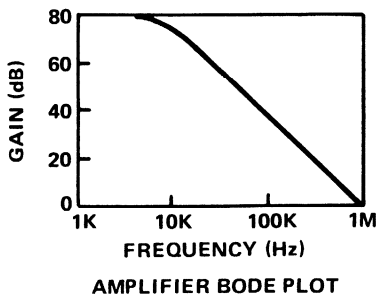flip-flop. The flip-flop is toggled on the trailing edge of the pulse width modulated signal gating it to each of the outputs alternately; therefore, the switching frequency of each output is one-half the oscillator frequency.

The output control (pin 13) must never be left open. It may be connected to the internal voltage reference (pin 14) or ground (pin 7).

Output Driver Stages

The two identical Darlington output drivers may be operated in parallel or push-pull mode. Both the collector and emitter terminals are available for various drive configurations. $V_{CE(sat)}$ of each output at 200 mA is typically 1.1 V in common-emitter configuration and 1.5 V in common-collector configuration. These drivers are protected against overload but do not have sufficient current-limiting to be operated as current source outputs.

TL594 APPLICATION HINTS

Soft-Start

Use of a soft-start protection circuit is recommended. This circuit prevents current surges during power-up and protects against false signals which might be created by the control circuit when power is applied.

Implementing a soft-start circuit is relatively simple using the dead-time control input (pin 4). Figure 6–13 shows an example.
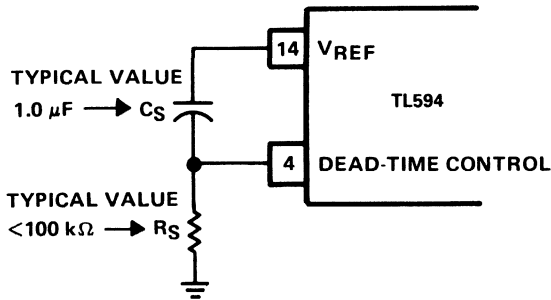
Fig. 6–13   Soft-Start Circuit.

Initially, capacitor C_S forces the dead-time control input to follow the internal 5 V reference which disables both outputs (100% dead time). As the capacitor charges through R_S, the output pulse width increases until the control loop takes command.

Over-Voltage Protection

The dead-time control input (pin 4) also provides a convenient input for over-voltage protection, which may be sensed as an output voltage condition, or input voltage protection as shown in Figure 6–14.
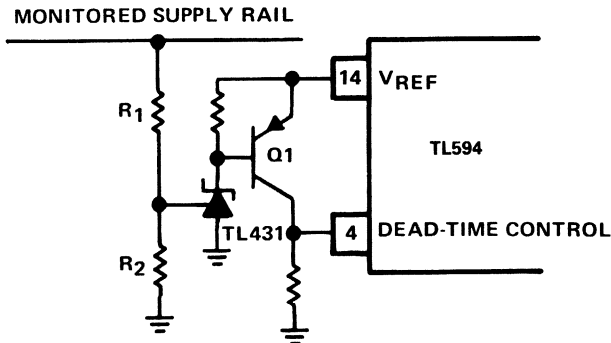
Fig. 6–14   Over-Voltage Protection Circuit.

A TL431 is used as the sensing element. When the monitored supply rail voltage increases to the point that 2.5 V is developed across R2, the TL431 conducts, Q1 becomes forward biased, and the dead-time control is pulled up to the reference voltage which disables the output transistors.

APPLICATIONS USING TL594 SERIES CONTROL CIRCUITS.

1. Designing a Power Supply 5 Volt/10 Amp Output

Design Objective

The design criteria is as follows:

$V_O = 5$ V

$V_I = 32$ V

$I_O = 10$ A

$f = 20$ kHz Switching Frequency

$V_R = 100$ mV peak-to-peak (V_{ripple})

$\Delta I_L = 1.5$ A Inductor Current Change

Input Power Source

The 32 V dc power source for this supply uses a 120 V input, 24 V output transformer rated at 75 VA. The 24 V secondary winding feeds a full-wave bridge rectifier followed by a current limit resistor (0.3 ohm) and two filter capacitors, as shown in Figure 6–15.
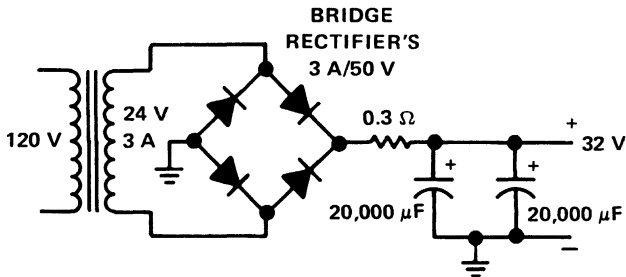
Fig. 6–15   Input Power Source.

The output current and voltage are determined by the following equations.

V rectifier = V secondary $\times \sqrt{2} = 24$ V $\times \sqrt{2} = 34$ V

$$I \text{ rectifier (avg)} \approx \left[\frac{V_O}{V_I} \right] \times I_O \approx \frac{5\,V}{32\,V} \times 10\,A \approx 1.6\,A$$

This assumes 100% efficiency. Assuming 70% efficiency:

$I \text{ rectifier (avg)} \approx 2.3A$

The 3 A/50 V full-wave bridge rectifier meets these calculated conditions. Figure 6–16 illustrates the switching and control section.
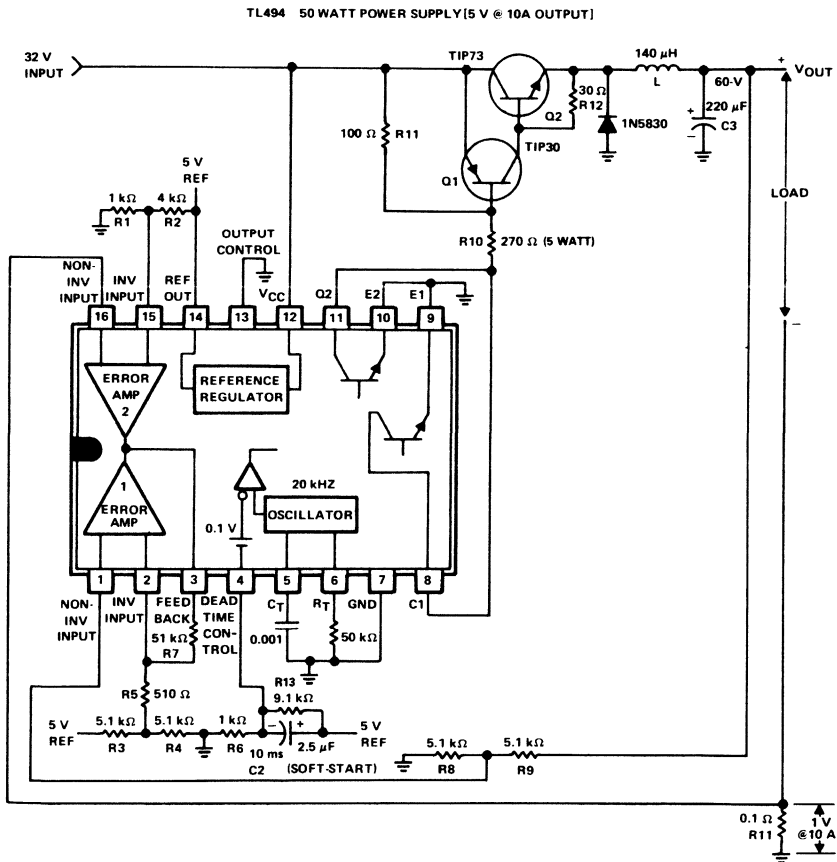
Fig. 6–16   Switching and Control Section.

Control Circuits

Oscillator

The TL594 oscillator frequency is controlled by connecting an external timing circuit consisting of a capacitor and resistor to pins 5 and 6. The oscillator is set to operate at 20 kHz using the component values calculated by the following equations.

$$f = \frac{1}{R_T C_T}$$

where:

R_T = Value of timing resistor

C_T = Value of timing capacitor

Choose $C_T = 0.001\ \mu F$ and calculate R_T.

$$R_T = \frac{1}{f \times C_T} = \frac{1}{20 \times 10^3 \times 0.001 \times 10^{-6}}$$

$$= 50\ k\Omega$$

Error Amplifier

The error amplifier compares a sample of the 5 V output to a reference and adjusts the pulse-width modulator to maintain a constant output as shown in Figure 6–17.
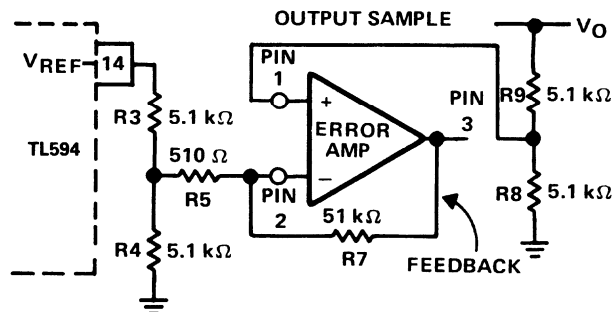
Fig. 6–17   Error Amplifier Section.

The TL594's internal 5 V reference (pin 14) is divided to 2.5 V by R3 and R4. The output voltage error signal is also divided to 2.5 V by R8 and R9. If the output must be regulated to exactly 5.0 V, a 10 kΩ potentiometer may be used in place of R8 to provide an adjustment control.

To increase the stability of the error amplifier circuit, the output of the error amplifier is fed back to the inverting input through R7, reducing the dc gain to 100.

Current Limit Amplifier

The power supply was designed for a 10 A load current and an I_L swing of 1.5 A; therefore, the short circuit current should be

$$I_{SC} = I_O + \frac{I_L}{2} = 10.75 \text{ A}$$

The current limit portion of the circuit is shown in Figure 6–18. The power supply was designed for a 10 A load current. Resistors R1 and R2 set a reference of about 1 V on the inverting input of the current limit amplifier. Resistor R11, in series with the load, applies 1 V to the non-inverting terminal of the current limit amplifier when the load current reaches 10 A. The output pulse width will be reduced accordingly. The value of R11 is calculated as follows:

$$R11 = \frac{1 \text{ V}}{10 \text{ A}} = 0.1 \text{ }\Omega$$
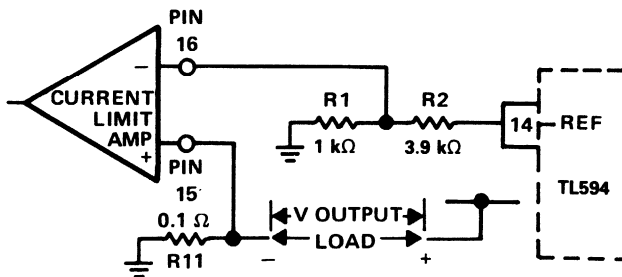
Fig. 6–18   Current Limit Circuit.

Soft-Start and Dead Time

To reduce stress on the switching transistors at startup, the startup surge which occurs as the output filter capacitor charges, must be reduced. The availability of the dead-time control makes implementation of a soft-start circuit, as shown in Figure 6–19, relatively simple.
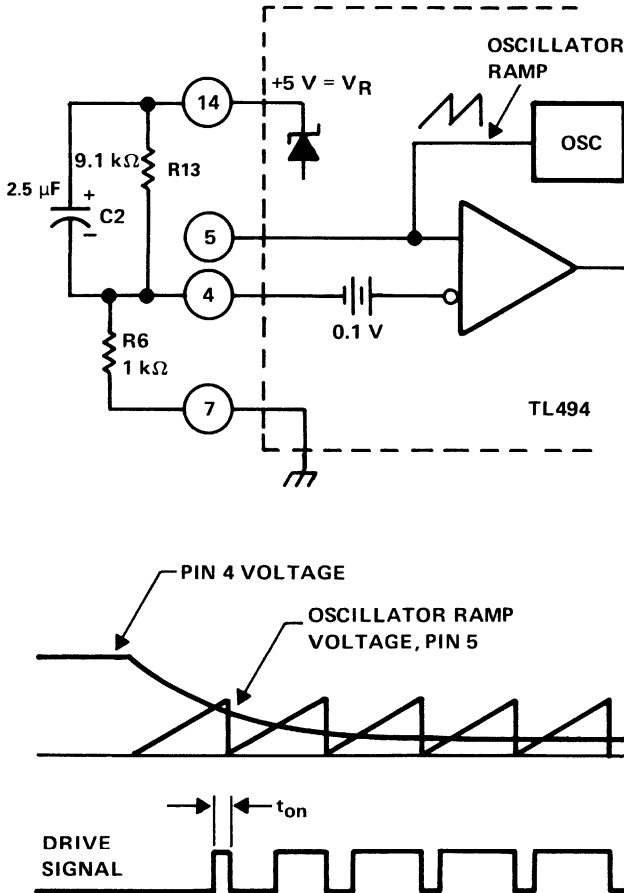
Fig. 6–19   Soft-Start Circuit.

The 'soft-start' circuit allows the pulse width at the output to increase slowly, as shown in Figure 6–19, by applying a negative slope waveform to the dead-time control input (pin 4).

Initially, capacitor C2 forces the dead-time control input to follow the 5 V reference regulator, which disables the outputs (100% dead time). As the capacitor charges through R6, the output pulse width slowly increases until the control loop takes command. With a resistor ratio of 1:9 for R6 and R13 the voltage at pin 4 after start up will be 0.1 × 5 V limiting the maximum duty cycle to 83%.

The soft-start time is generally in the range of 25 to 100 clock cycles. If we select 50 clock cycles at a 20 kHz switching rate, the soft start time is calculated as follows:

$$T = \frac{1}{f} = \frac{1}{20\,kHz} = 50\,\mu s \text{ per clock cycle}$$

The value of the capacitor is then determined by

$$C2 = \frac{\text{soft start time}}{R6} = \frac{50\,\mu s \times 50\,\text{cycles}}{1\,k\Omega}$$

$$= 2.5\,\mu F$$

This helps to eliminate any false signals which might be created by the control circuit as power is applied.

Inductor Calculations

The switching circuit used is shown in Figure 6–20.

INDUCTOR CALCULATIONS
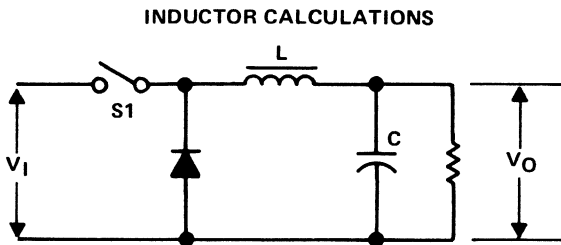
Fig. 6–20   Switching Circuit.

The size of the inductor (L) required is calculated as follows:

$$d = \text{Duty Cycle} = \left(\frac{V_O + V_F}{V_I + V_F} \right) = \frac{6\text{ V}}{33\text{ V}} = 0.182$$

where V_F is rectifier forward volt drop.

$$f = 20\text{ kHz (Design Objective)}$$

$$t_{on} = \text{time on (S1 closed)} = \frac{1}{f} \times d = 9.1\ \mu s$$

$$t_{off} = \text{time off (S1 open)} = \frac{1}{f} - t_{on} = 40.9\ \mu s$$

$$L \approx \frac{(V_I - V_O) \times t_{on}}{\Delta I_L} \approx \frac{(32\text{ V} - 5\text{ V}) \times 9.1\ \mu s}{1.5\text{ A}}$$

$$\approx 163.8\ \mu H$$

$$L \approx 165\ \mu H$$

Output Capacitance Calculations

Once the filter inductance has been calculated, the value of the output filter capacitor is calculated to meet the output ripple requirements. An electrolytic capacitor can be modelled as a series connection of an inductance, a resistance, and a capacitance. To provide good filtering, the ripple frequency must be far below the frequencies at which the series inductance becomes important; so, the two components of interest are the capacitance and the effective series resistance (ESR). The maximum ESR is calculated according to the relation between the specified peak-to-peak ripple voltage and peak-to-peak ripple current.

$$\text{ESR(max)} = \frac{\Delta V_{O(ripple)}}{\Delta I_L} = \frac{0.1\text{ V}}{1.5\text{ A}} = 0.067\ \Omega$$

The minimum capacitance of C3 necessary to maintain the V_O ripple voltage at less than the 100 mV design objective was calculated according to the following equation.

$$C3 = \frac{\Delta IL}{8\,f\Delta V_O} = \frac{1.5\ A}{8 \times 20 \times 10^3 \times 0.1\ V} = 94\ \mu F$$

A capacitor should be selected that has an ESR less than 0.067 Ω.

Transistor Power Switch Calculations

The transistor power switch was constructed with a TIP30 pnp drive transistor and a TIP73 npn output transistor. These two power devices were connected in a pnp hybrid Darlington circuit configuration as shown in Figure 6–21.
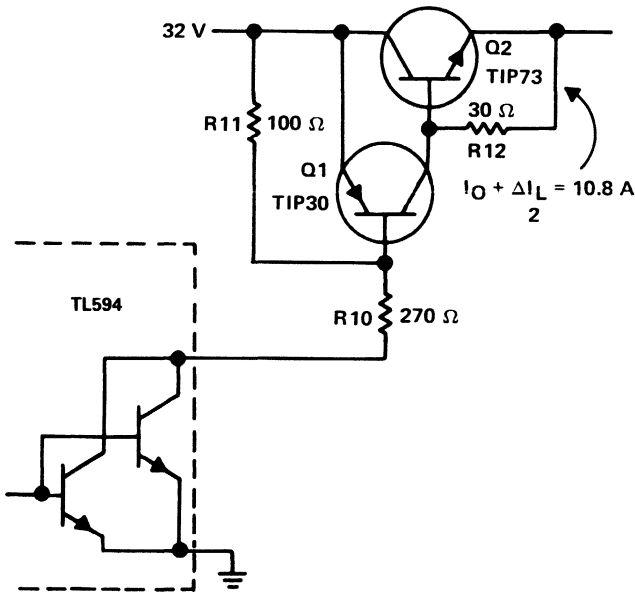
Fig. 6–21   Power Switch Section.

The hybrid Darlington must be saturated at a maximum output current of $I_O + \Delta I_L/2$ or 10.8 A. The Darlington h_{FE} at 10.8 A must be high enough not to exceed the 250 mA maximum output collector current of the TL594. Based on published TIP30 and TIP73 h_{FE}

specifications, the required power switch minimum drive was calculated by the following equations to be 108 mA.

$$h_{FE}(Q1) \text{ at } I_C \text{ of } 1.2 \text{ A} = 10$$

$$h_{FE}(Q2) \text{ at } I_C \text{ of } 12.0 \text{ A} = 10$$

$$i_B \geqslant \frac{I_O + \frac{\Delta I_L}{2}}{h_{FE}(Q2) \times h_{FE}(Q1)} \geqslant 108 \text{ mA}$$

The value of R10 was calculated by the following equation.

$$R10 \leqslant \frac{V_1 - (V_{BE}(Q1) + V_{CE}(TL594))}{i_B}$$

$$= \frac{32 - (1.3 + 0.7)}{0.108}$$

$$R10 \leqslant 277 \ \Omega$$

Used on these calculations, the nearest standard resistor value of 270 Ω was selected for R10. Resistors R11 and R12 permit the discharge of carriers in the switching transistors when they are turned off.

The power supply described demonstrates the flexibility of the TL594 pulse-width-modulation control circuit.

2. Floppy Disk Power Supply

The TL593 incorporates, on a single monolithic chip, all the functions required for a pulse-width modulation control circuit. Figure 6–22 shows the schematic for a floppy disk power supply. It uses a TL593 and is similar to the TL594, from which it was derived, except that the TL593 includes a current-limit amplifier instead of a second error amplifier. The current-limit amplifier of the TL593 has an offset voltage of approximately 80 mV in series with the inverting input (pin 15). This makes it easier to design the current-limit portion of the power supply and also requires fewer components. With 80 mV on the
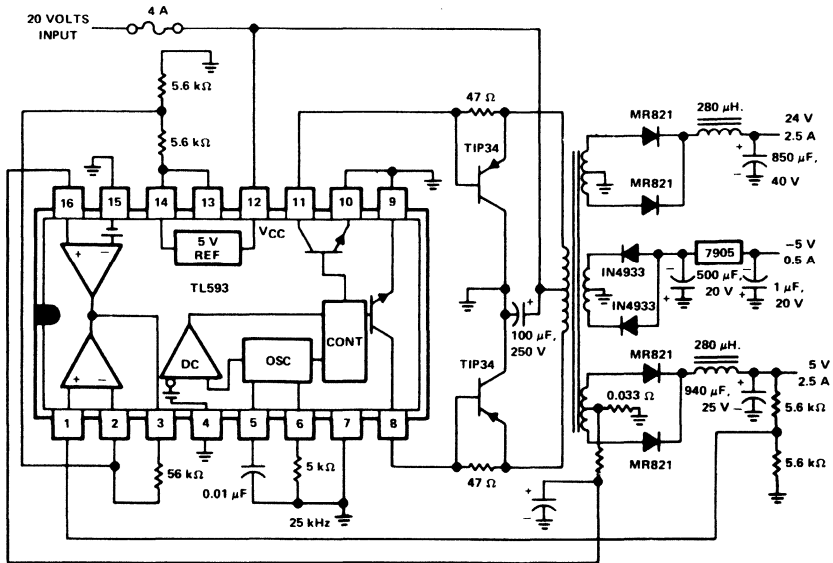
Fig. 6–22   TL593 Floppy Disk Power Suppy.

inverting input, it is only necessary to apply an 80 mV control voltage to the non-inverting input (pin 16) in order to current limit the output. This is easily accomplished by sensing the voltage across a resistor in series with the load.

The power supply uses a pair of TIP34 pnp transistors in a push-pull configuration. The oscillation frequency is set at 25 kHz by the .01 μF capacitor on pin 5 and the 5 kΩ resistor on pin 6.

The centre connection of the two 5.6 kΩ resistors on pins 13 and 14 establishes a 2.5 V reference voltage on pin 2, which is the inverting input of the voltage control error amplifier. The voltage feedback to pin 1, the non-inverting input, is biased from the center connection of the two 5.6 kΩ resistors located across the 5 V/2.5 A power supply output terminal. Because this voltage supplies the logic circuits, it requires closer regulation than the auxiliary outputs.

The 24 V winding, on the other hand, is not critical as it furnishes voltage for the stepping motor. The −5 V supply is regulated separately with a uA7905 three-terminal regulator.

In choosing components for this circuit, the same precautions taken in the construction of any switching power supply should be observed; be careful of layout, ground loops, and heatsinking of the power transistors. In the output section, where high frequency rectifiers are needed, either Schottky or fast recovery diodes should be used. For output capacitors, low equivalent series resistance (ESR) types should be used. The output ripple depends more on the resistance than on the capacitance value.

Transformer Construction

The transformer for this circuit was wound on a toroid core. The core used was 3C8 ferrite material (F–42908–TC).

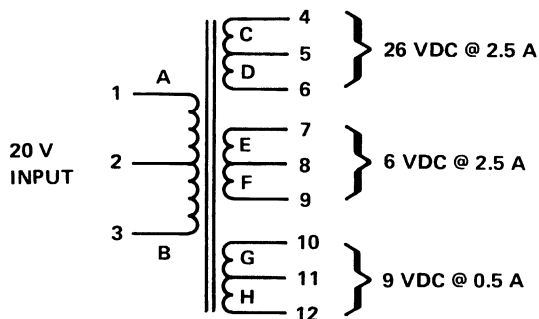The winding layout is shown in Figure 6–23.

Fig. 6–23   Transformer Winding Layout.

Transformer Winding Data

Primary A + B = 28 turns bifilar #20 HNP

Secondary C + D = 28 turns bifilar #20 HNP over A + B

Secondary E + F = 6 turns bifilar #20HNP over C + D

Secondary G + H = 10 turns bifilar #26 HNP over E + F

NOTE: All windings to be centre tapped.

DC Resistance

Winding 1 – 3 = 0.11 Ω

Winding 4 – 6 = 0.11 Ω

Winding 7 – 9 = 0.025 Ω

Winding 10 – 12 = 0.15 Ω

3. TL594 12–VOLT TO 5–VOLT STEP-DOWN BUCK REGULATOR

The TL594 switching voltage regulator operates as a step-down converter in a continuous mode. It the output current falls below a specified minimum value the inductor current becomes discontinuous. The main advantages of a step-down converter in the continuous mode are:—

1. The ripple voltage at the output can be kept low, even in high current designs.

2. The ratio of peak current in the switching device to output is determined by the inductor value and is typically low. For a specific output current requirement, the current rating for the switching transistor can be lower than for a transistor operating in a discontinuous mode.

3. Pulse-width modulation occurs with input voltage variations. Load variations are compensated for by modulation of the dc current level in the inductor, as well as by pulse-width modulation. This allows high efficiency to be maintained over the entire load range (from I_o max to I_o min).

The disadvantages of this type of converter are:

1. The inductance value required may result in a large component size.

2. Transient response is impaired by high inductance values.

3. Although peak current in the rectifier is reduced, losses due to reverse recovery current are increased.

The complete circuit for the TL594 Step-down Regulator is shown in Figure 6–24.
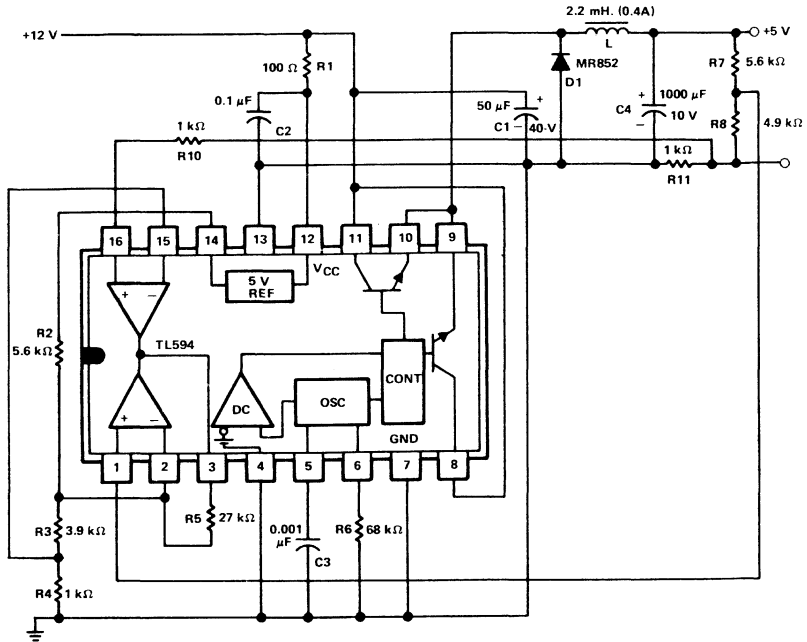
Fig. 6–24   TL594 12-Volt Step-Down Regulator.

For this application the two switching transistors operate in phase with each other by grounding the output control, pin 13. The switching transistors supply input to the inductor, L, for part of the oscillator cycle. For the remaining part of the oscillator cycle the voltage across the inductor reverses and diode D1 starts conducting, maintaining current flow in the inductor while the transistors are off (see Figure 6–25).

The input supply through R1 to pin 12 is decoupled by capacitor C2. Capacitor C4 filters the output voltage. The timing components C3 and R6 set the oscillator frequency to 15 kHz. The 2.2 mH inductor can be made on an RM7 ferrite core with 94 turns of #28 transformer wire.

Output current limiting of 500 mA is provided by sensing the overcurrent output with R11 and feeding the resultant error voltage to the positive input of the current error amplifier on pin 16. The negative input to this error amplifier is biased to 500 mV from reference divider R2, R3 and R4.

This resistor network also furnishes about 2.3 V bias to the voltage control error amplifier on pin 2. An output error voltage signal is taken from the junction of R7 and R8 and fed to the positive input of the voltage control error amplifier on pin 1. The voltage control loop gain is set by feedback resistor R5.
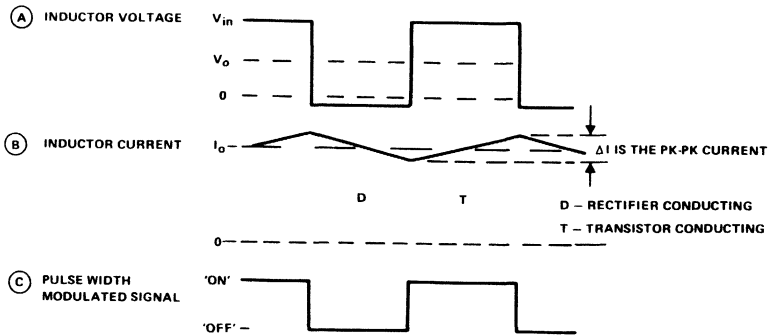
Fig. 6–25   12–Volt to 5-Volt Series Switching Regulator Waveforms.

Specifications

Input Voltage	12 V nominal
	(10 V to 15 V)
Output Voltage	5 V ±10%
Output Ripple	50 mV$_{pp}$
Output Current	400 mA
Output Power	2 W at 5 V output
Short Circuit Protection	500 mA constant current
Efficiency	typically 70%

APPLICATIONS USING TL497A SWITCHING VOLTAGE REGULA- TOR

The TL497A is a fixed-on-time, variable-frequency voltage regulator controller. The block diagram of the TL497A is shown in Figure 6–26.
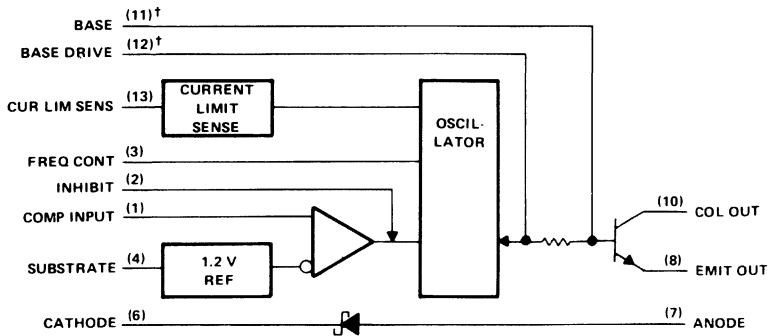
†The Base pin (#11) and Base Drive pin (#12) are used for device testing only. They are not normally used in circuit applications of the device. Supply pin is Pin 14.

Fig. 6–26   TL497A Block Diagram.

The on-time is controlled by an external capacitor connected between the frequency control pin (pin 3) and ground. This capacitor. C_T, is charged by an internal constant-current generator to a predetermined threshold. The charging current and threshold vary proportionately with V_{CC}; thus, the on-time remains constant over the allowable input voltage range.

The output voltage is controlled by two series resistors in parallel with the supply output. The resistance ratio is calculated to supply 1.2 V to the comparator input (pin 1) with respect to pin 4 at the desired output voltage. This feedback voltage is compared to the 1.2 V bandgap reference by the high-gain error amplifier. When the output voltage falls below the desired voltage, the error amplifier enables the oscillator circuit, which charges and discharges C_T.

The npn output transistor is driven 'on' during the charging cycle of C_T. The internal transistor can switch currents up to 500 mA. It is current driven to allow operation in either emitter follower or common emitter configuration. An internal diode matched to the current characteristics of the output transistor is included on the chip and may be used for blocking or commutating purposes.

The TL497A also contains current-limiting circuitry which senses the peak currents in the switching regulator and protects the inductor against saturation and the output transistor against overstress. The

current limit is adjustable and is set by a single sense resistor between pins 13 and 14. The current-limit circuitry is activated when 0.5 V is developed across current-limit resistor R_{CL}.

The TL497A contains all the active elements required for constructing a single-ended dc-to-dc converter. The output transistor and the rectifier are uncommitted allowing maximum flexibility in the choice of circuit configuration.

The TL497A's primary feature is design simplicity. Using six external components; three resistors, two capacitors, and one inductor, the step-up, step-down, and inverting (requires use of an external rectifier diode) power supplies shown in Figure 6–27 may be constructed.

STEP DOWN	STEP-UP	INVERTING
POS → POS	POS → POS	POS → NEG
$+V_I > +V_O$	$+V_O > +V_I$	$+V_I > -V_O$
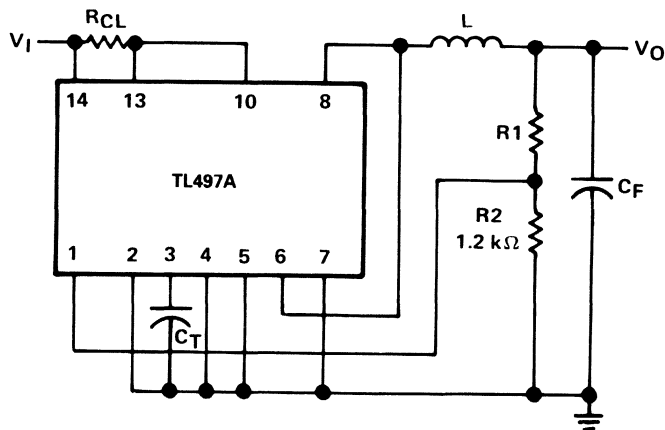
STEP DOWN

POS → POS

$(+) V_I > (+) V_O$

Fig. 6–27 a   Basic Power Supply Configurations.
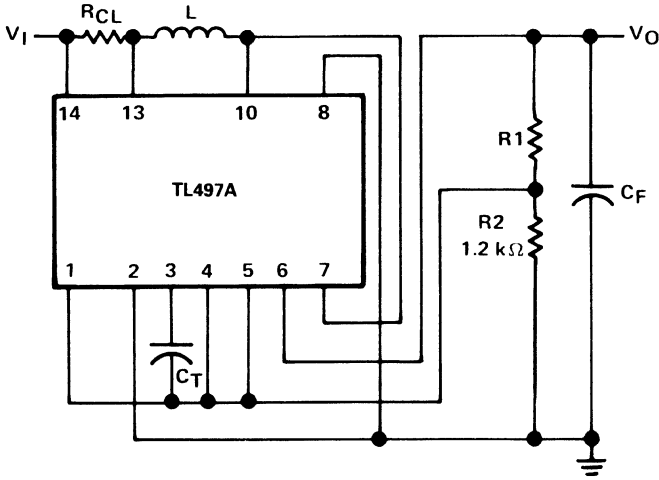
STEP UP

POS → POS

(+ V$_O$> (+) V$_I$

Fig. 6–27 b   Basic Power Supply Configurations.
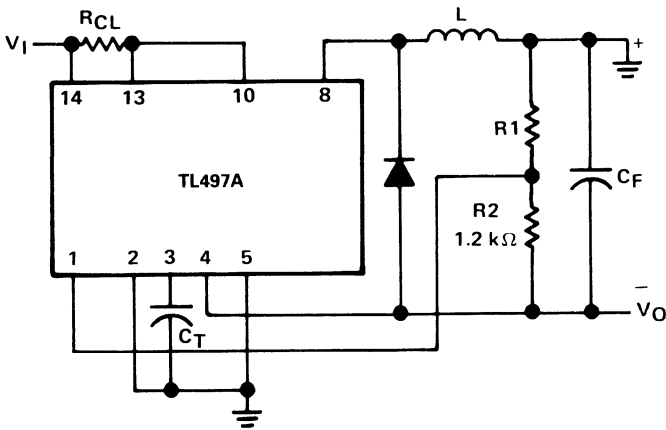
INVERT

POS → NEG

V + → V −

Fig. 6–27 c   Basic Power Supply Configurations.

Step-Down Switching Regulator

The circuit in Figure 6–28(a) illustrates the basic configuration for a step-down switching regulator.

When switch S1 is closed, the current in the inductor and the voltage across the capacitor start to build up. The current increases while switch S1 is closed as shown by the inductor waveform in Figure 6–28(b). The peak current in the inductor is dependent on the time S1 is closed (t_{on}).

When S1 opens, the current through the inductor is I_{pk}. Since the current cannot change instantaneously, the voltage across the inductor inverts, and the blocking diode (D1) is foward biased providing a current path for the discharge of the inductor into the load and filter capacitor. The inductor current discharges linearly as illustrated in Figure 6–28b.
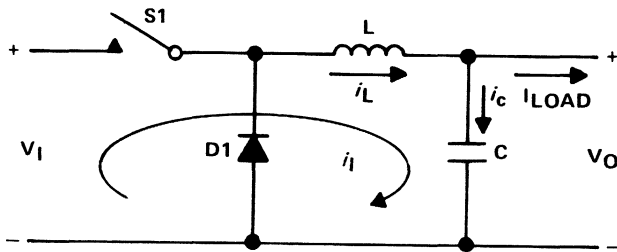
(a) BASIC STEP-DOWN REGULATOR
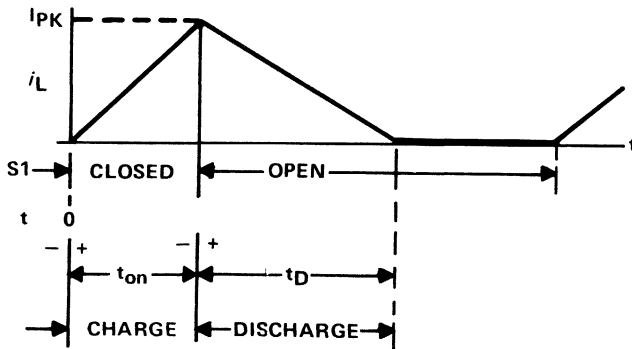
(b) INDUCTOR CURRENT WAVEFORM

Fig. 6–28   Step-Down Switching Regulator.

For the output voltage to remain constant, the net charge delivered to the filter capacitor must be zero. The charge delivered to the capacitor from the inductor must be dissipated in the load. Since the charge developed in the inductor is fixed (constant on-time), the time required for the load to dissipate that charge will vary with the load requirements. It is important to use a filter capacitor with minimal ESR. Note, however, some ripple voltage is required for proper operation of the regulator.

Figure 6–29 shows a positive, step-down configuration both with and without an external pass transistor. Design equations for calculating the external components are included.

DESIGN EQUATIONS
- $I_{PK} = 2\ I_{LOAD}\ max$
- $L\ (\mu H) = \dfrac{V_I - V_O}{I_{PK}}\ t_{on}\ (\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (20 to 150 μs)

- $C_T\ (pF) \approx 12\ t_{on}\ (\mu s)$
- $R1 = (V_O - 1.2)\ k\Omega$
- $R_{CL} = \dfrac{0.5\ V}{I_{PK}}$
- $C_F = \dfrac{(I_{PK} - I_{LOAD})^2}{(V_{ripple})\ 2\ I_{PK}} \times \dfrac{t_{on}\ V_I}{V_O}$

BASIC CONFIGURATION

$I_{PK} < 500$ mA)
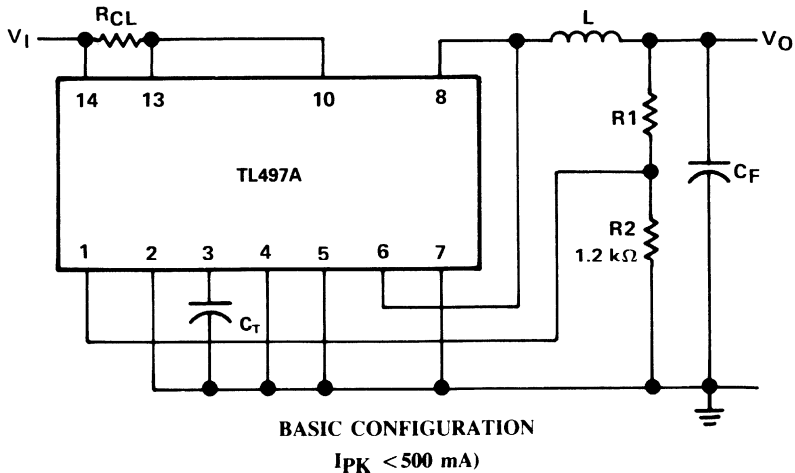
Fig. 6–29 a   Positive Regulato , Step-Down Configurations.

EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)
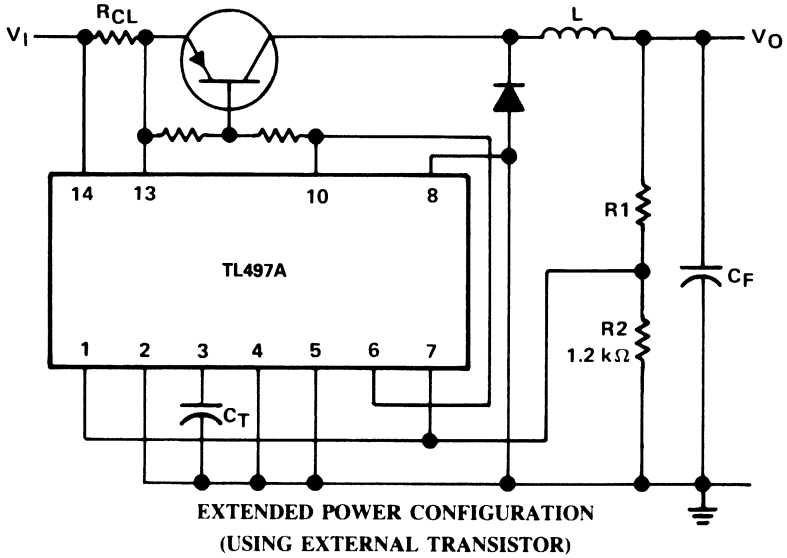
Fig. 6–29 b   Positive Regulator, Step-Down Configurations.
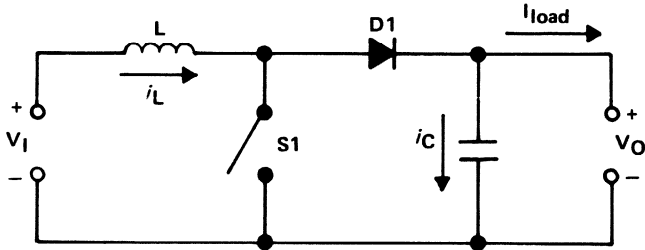
(a) BASIC STEP-UP REGULATOR CIRCUIT
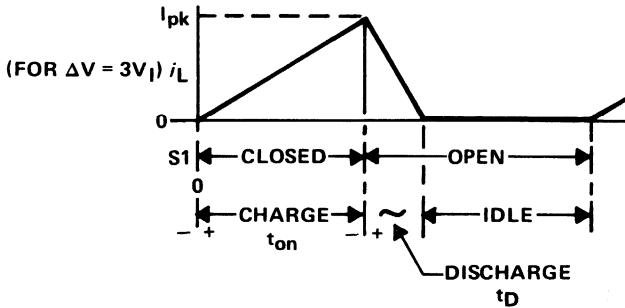
(b) INDUCTOR CURRENT WAVEFORM

Fig. 6–30   Step-Up Switching Regulator.

Step-Up Switching Regulator

In the step-up regulator, the formulae change slightly. During the charging cycle (S1 closed) the inductor (L) is charged directly by the input potential. The peak current is not related to the load current as it was in the step-down regulator because during the inductor charge cycle the blocking diode D1 is reverse-biased and no charge is delivered to the load.

The circuit in Figure 6–30(a) delivers power to the load only during the discharge cycle of the inductor (S1 open). The diode (D1) is forward biased and the inductor discharges into the load capacitor. Figure 6–31 shows a positive, step-down configuration both with and without an external pass transistor. Design equations are included.

DESIGN EQUATIONS

- $I_{PK} = 2\, I_{LOAD}\, max \left[1 + \dfrac{V_O}{V_I}\right]$

- $L\,(\mu H) = \dfrac{V_I}{I_{PK}}\, t_{on}(\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (25 to 150 μs)

- $C_T\,(pF) \approx 12\, t_{on}(\mu s)$
- $R1 = (V_O - 1.2)\, k\Omega$
- $R_{CL} = \dfrac{0.5\,V}{I_{PK}}$

- $C_F = \dfrac{(I_{PK} - I_{LOAD})^2}{(V_{ripple})\, 2\, I_{PK}} \times \dfrac{t_{on}\, V_I}{V_O}$

BASIC CONFIGURATION

(I_{PK} < 500 mA)

Fig. 6–31 a   Positive Regulator, Step-Up Configurations.

EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

Fig. 6–31 b   Positive Regulator, Step-Up Configurations.

Inverting Configuration

The inverting regulator is similar to the step-up regulator. During the charging cycle of the inductor the load is isolated from the input. The only difference is in the potential across the inductor during its discharge. This can best be demonstrated by a review of the basic inverting regulator circuit (6–32).
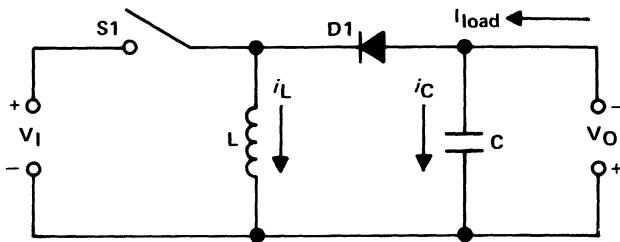
Fig. 6–32   Basic Inverting Regulator Circuit.

During the charging cycle (S1 closed) the inductor (L) is charged only by the input potential, similar to the step-up configuration. In the inverting configuration the input provides no contribution to the load current during the charging cycle. The maximum load current for discontinuous operation will be limited by the peak current, as observed in the step-up configuration. The inductor current waveform looks identical to the waveform demonstrated in the step-up configuration [see Figure 6–30(b)].

Figure 6–33 shows the inverting applications both with and without an external pass transistor. Design equations are also included.

DESIGN EQUATIONS

- $I_{PK} = 2\, I_{LOAD}\, max\left[1 + \dfrac{V_O}{V_I}\right]$

- $L\,(\mu H) = \dfrac{V_I}{I_{PK}}\, t_{on}\,(\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (25 to 150 μs)

- $C_T\,(pF) \approx 12\, t_{on}\,(\mu s)$

- $R2 = (V_O - 1.2)\, k\Omega$

- $R_{CL} = \dfrac{0.5\ V}{I_{PK}}$

- $C_F = \dfrac{(I_{PK} - I_{LOAD})^2}{(V_{ripple})\, 2\, I_{PK}} \times \dfrac{t_{on}\, V_I}{V_O}$
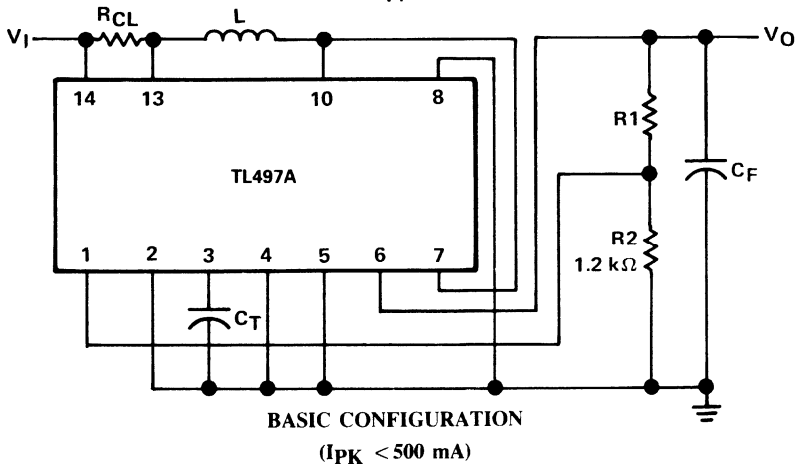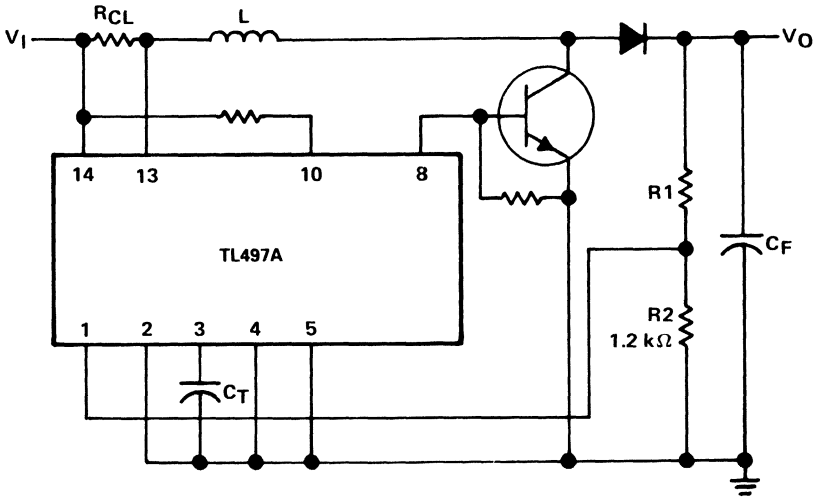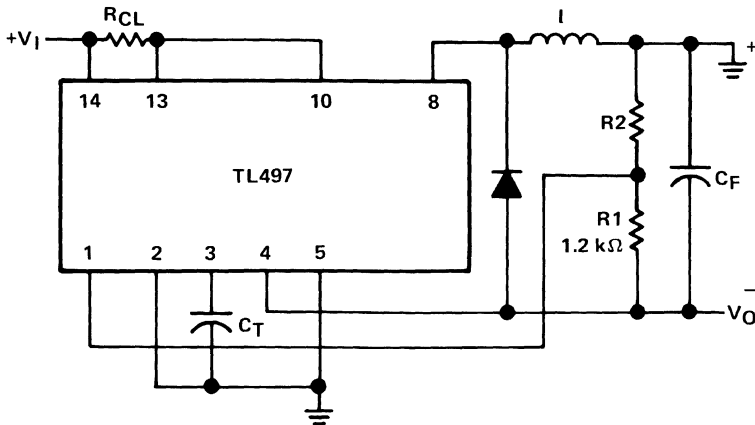

BASIC CONFIGURATION

(I_{PK} < 500 mA)

Fig. 6–33 a   Inverting Applications.
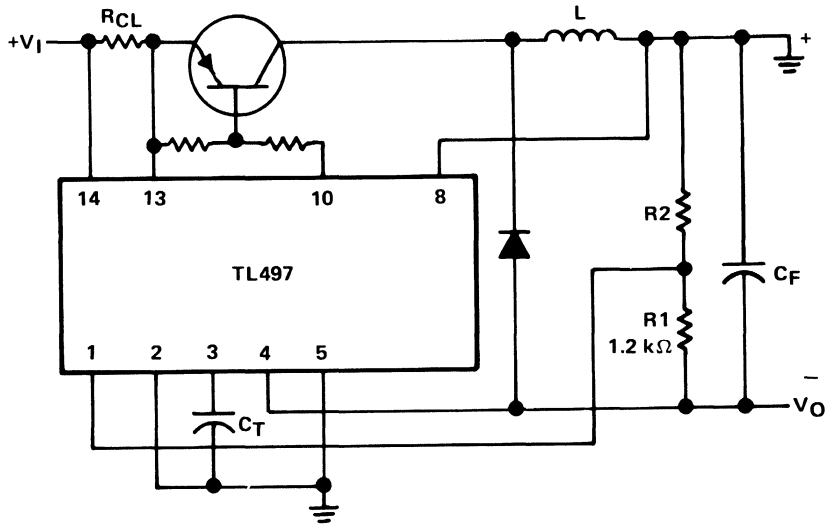
EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

Fig. 6–33 b   Inverting Applications.

Note that in the inverting configuration the internal diode is not used. An external diode must be used because pin 4 (substrate) must be the most negative point on the chip. The cathode of the internal diode is also the cathode of a diode connected to the substrate. When the cathodes are at the most negative voltage in the circuit, there will be conduction to the substrate resulting in unstable operation.

Design Considerations

An oscilloscope is required when building a switching regulator. When checking the oscillator ramp on pin 3 of the TL497A the oscilloscope may be difficult to synchronize. This is a normal operating characteristic of this regulator and is caused by the asynchronous operation of the oscillator. The oscilloscope may be synchronized by varying the input voltage or load current slightly from design nominals.

High frequency circuit layout techniques are imperative. Keep leads as short as possible and use a single ground point. Resistors R1 and R2 should be as close as possible to Pin 1 to eliminate noise pick-up

in the feedback loop. The TL497A type of circuits do not need 'hi-Q' inductors. They are, in fact, not desirable due to the broad frequency range of operation. If the 'Q' is too high, ringing will occur. If this happens a shunt resistor (about 1 kΩ) may be placed across the coil to damp the oscillation.

While not necessary, it is highly desirable to use a toroidal inductor as opposed to a cylindrically wound coil. The toroidal type of winding helps to contain the flux closer to the core and in turn minimize radiation from the supply. All high current loops should be kept to a minimum length using copper connections that are as large as possible.

A STEP-DOWN SWITCHING REGULATOR DESIGN EXERCISE WITH TL497A

The schematic of a basic step-down regulator is shown in Figure 6–34.
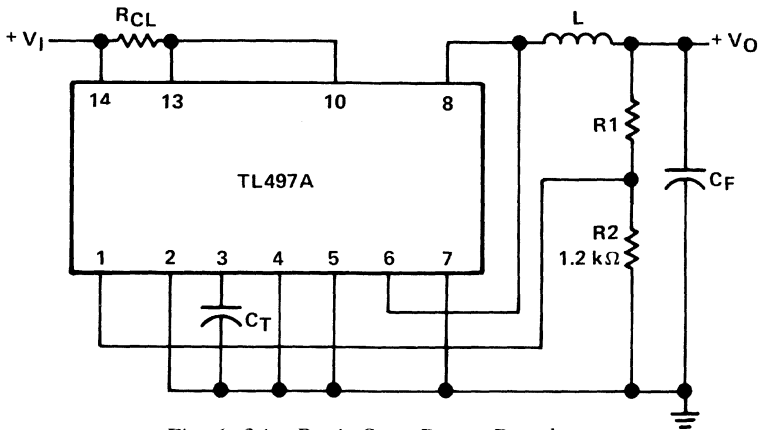
Fig. 6–34   Basic Step-Down Regulator.

This regulator will have the following design goals:

$$V_I = 15\ V$$

$$V_O = 5\ V$$

$$I_O = 200\ mA$$

$$V_{ripple} = < 1.0\%\ or\ 50\ mV\ (1.0\% \times 5\ V)$$

Calculations:

$I_{PK} = 2\, I_L\, max = 400\, mA$

For design margin, I_{PK} will be designed for 500 mA which is also the limit of the internal pass transistor and diode.

$\therefore I_{PK} = 500\, mA$

The next step will be to select t_{on}. You may select a timing capacitor to match an inductor you may already have. You may also assume an on-time and calculate the inductor value. We will assume an on-time of 20 μs.

$t_{on} = 20\, \mu s$

$$L(\mu H) = \frac{V_I - V_O}{I_{PK}} \times t_{on}\ \mu s$$

$$= \frac{15 - 5}{0.5} \times 20 = 400\ \mu H$$

$L = 400\ \mu H$

To set the TL497A for 5 V output:

$R2 = 1.2\, k\Omega$ (fixed)

$R1 = (5 - 1.2)\, k\Omega = 3.8\, k\Omega$

To set current limiting:

$$R_{CL} = \frac{0.5}{I_L} = \frac{0.5}{500 \times 10^{-3}} = 1\ \Omega$$

$R_{CL} = 1\ \Omega$

For the on-time chosen, C_T can be approximated:

$C_T(pF) = 12\, t_{on}\ \mu s$

$C_T \qquad = 240\, pF$

or it may be selected from a table in the data sheet.

To determine filter capacitor (C_F) for desired ripple voltage:

$$C_F = \frac{(I_{PK} - I_L)^2}{(V_{ripple})\, 2\, I_{PK}} \times \frac{t_{on}\, V_I}{V_O}$$

$$C_F = \frac{(0.5 - 0.2)^2}{(0.05)\, 2 \times 0.5} \times \frac{20 \times 10^{-6} \times 15}{5}$$

$$= 108\ \mu F$$

C_F was selected to be 120 μF, the next higher preferred value.

Figure 6–35 illustrates the regulator with the calculated values applied to it.
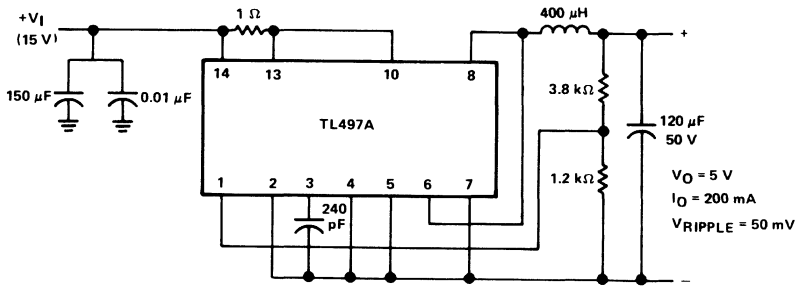
Fig. 6–35   15-Volt to 5-Volt Step-Down Regulator.

A 150 μF filter capacitor may be used as a prefilter as well as a 0.01 μF disc capacitor to take care of any transients on the incoming V_I rail.

For peak currents greater than 500 mA, it is necessary to use an external pass transistor and diode. Such a technique is illustrated in Figure 6–36 which is an automotive power supply. With a 12 V battery, this step-down regulator supplies 5 V at 2 A output current.

Figure 6–37 illustrates a basic step-up regulator. This design steps up the output voltage from 5 V to 15 V. The equations for determining the values of the external components are provided in Figure 6–31.
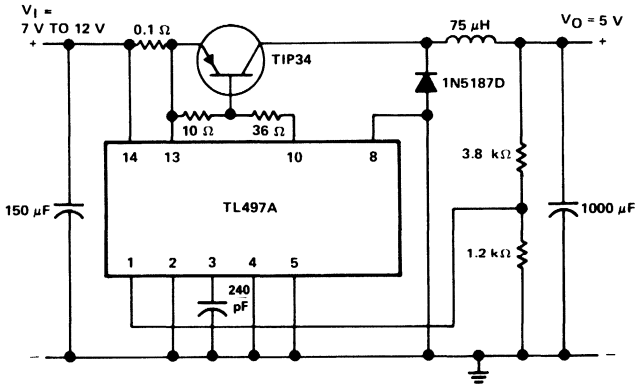
Fig. 6–36   Step-Down Regulator.
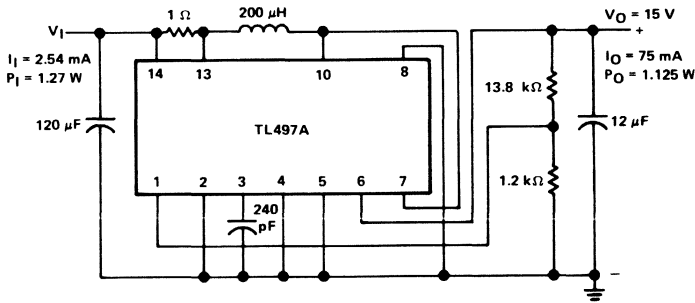
Fig. 6–37   5-Volt Switching Regulator.

DESIGN AND OPERATION OF AN INVERTING REGULATOR

Figure 6–38 illustrates a basic inverting regulator designed to have – 5 V output with +5 V input using the design equations in Figure 6–33.

Conditions:

$$V_I = 5\,V$$

$$V_O = -5\,V$$

$$I_O = 100\,mA$$

$$V_{ripple} = 1.0\% \text{ or } 50\,mV\ (1\% \times 5\,V)$$
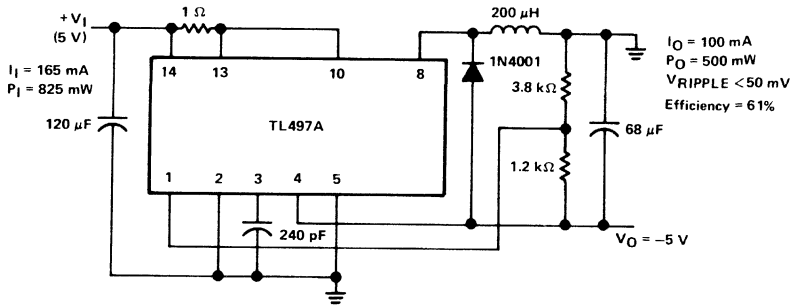
NOTE — Do not use internal diode (Pins 6, 7) on an inverting circuit.

Fig. 6–38   +5-Volt to −5-Volt Switching Regulator.

Calculations:

$$I_{PK} = 2\,I_L\,(\text{max})\left(1 + \frac{|V_O|}{V_I}\right)$$

$I_{PK} = 400\,\text{mA}$ (for design margin use $500\,\text{mA}$)

Assume $t_{on} = 20\,\mu s$

$$C_{T(pF)} = 12\,t_{on}(\mu s)$$

$$C_T = 240\,\text{pF}$$

$$L = \frac{V_I}{I_{PK}}\,t_{on} = \frac{5}{0.5} \times 20 = 200\,\mu H$$

To set the output voltage:

R2 = 1.2 kΩ

R1 = (5 − 1.2) kΩ = 3.8 kΩ

To set the current limiting:

$$R_{CL} = \frac{0.5}{I_{PK}} = \frac{0.5}{0.5}$$

$R_{CL} = 1\,\Omega$

To determine C_F for desired ripple voltage:

$$C_F = \frac{(I_{PK} - I_L)^2}{(V_{ripple})\, 2I_{PK}} \times \frac{t_{on}\, V_I}{|V_O|}$$

$$= \frac{(0.5 - 0.1)^2}{(0.05)\, 2 \times 0.5} \times \frac{20 \times 10^{-6} \times 5}{|-5|}$$

$C_F = 64\ \mu F$ (nearest standard value $= 68\ \mu F$)

Section 7

Power Supply Supervision and Protection

As electronic equipment becomes more sophisticated there is an increasing need for independent power supply supervision and protection. Under voltage conditions can cause corruption of data in micro-computer and other logic systems. Since the result can be dramatic and sometimes dangerous the use of a supply voltage supervisor is becoming normal practice.

Similarly the need to protect against accidental overstress is also becoming standard design practice,

The subject of this section is the description and application of dedicated integrated circuits which provide relatively easy solutions to the above.

SUPPLY VOLTAGE SUPERVISOR

After POWER-ON a digital system must normally be forced into a definite intitial state. For microcomputers and microprocessors a RESET input is provided to which, in simple applications, an R/C network is connected. After POWER-ON, this circuitry maintains the logic level at this input HIGH (or LOW), until the supply voltage has reached its nominal value, and the internal logic of the microcomputer has executed the RESET.
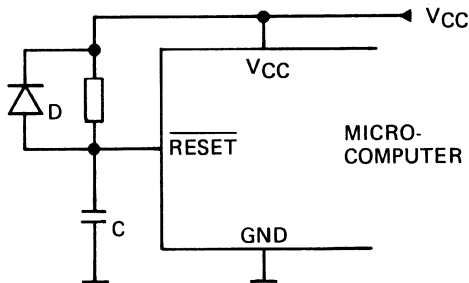
Fig. 7–1   RESET circuit.

However, this circuit does not work well during short drops of the supply voltage. In this case, the capacitor C must be quickly discharged via the diode D, which will occur only if the supply voltage V_{CC} goes below the threshold voltage (1 to 2 Volts) of the RESET input. A small decrease of V_{CC} under the recommended supply voltage can destroy the content of the memory and registers and yet not activate the RESET circuit. This may have 'catastrophic' consequences.

The following program example (8080 assembler code) tests an input:

```
WAIT   LXI      B, INPUT     ; load address
LOOP   LDAX     B            ; read input
       ANI      MASK         ; mask bit
       JNZ      LOOP         ; test
```

If, during the execution of the loop, the content of the B register is affected by a short voltage drop (causing an incorrect input to be read), an incorrect condition will be tested and an incorrect decision will be the consequence. Alternatively the input addressed will show a value which can never give a positive test result: the execution of the program seems to be stopped.

In larger computers several features are provided to prevent such errors: a power-fail interrupt signals dangerous conditions in time, the content of the memory is protected by a battery back-up, and so on. In small microcomputer systems this amount of effort is too expensive, and in most applications also not required. It is usually sufficient if, after a serious voltage drop, the microcomputer is forced into a defined initial condition. To implement this function, whilst preventing the problems mentioned above, a circuit with the following features is required:

● Accurate detection of a serious voltage drop.

● Generation of a RESET signal as long as the supply voltage is not in the operational range, to prevent undefined operations of the microcomputer.

● Maintenance of the RESET signal for a certain time after the supply voltage has returned to its nominal value, to ensure a proper RESET.

For these applications, TEXAS INSTRUMENTS has developed a series of integrated circuits which, with a minimum of external components and without additional adjustment, will fulfill the requirements described above.

CIRCUIT DESCRIPTION

The most critical element of this circuit is the reference voltage source, which consists of a very stable, temperature compensated band gap reference. An external capacitor (typ. 0.1 μF) must be connected to the voltage output V_{ref}, to reduce the influence of fast transients in the supply voltage. The voltage at the SENSE input is divided by a resistor divider and compared with the reference voltage by a comparator.

NOTE A   TL7702A: R1 = 0Ω, R2 = open
         TL7705A: R1 = 7.8 kΩ, R2 = 10 kΩ
         TL7709A: R1 = 19.7 kΩ, R2 = 10 kΩ
         TL7712A: R1 = 32.7 kΩ, R2 = 10 kΩ
         TL7715A: R1 = 43.4 kΩ, R2 = 10 kΩ
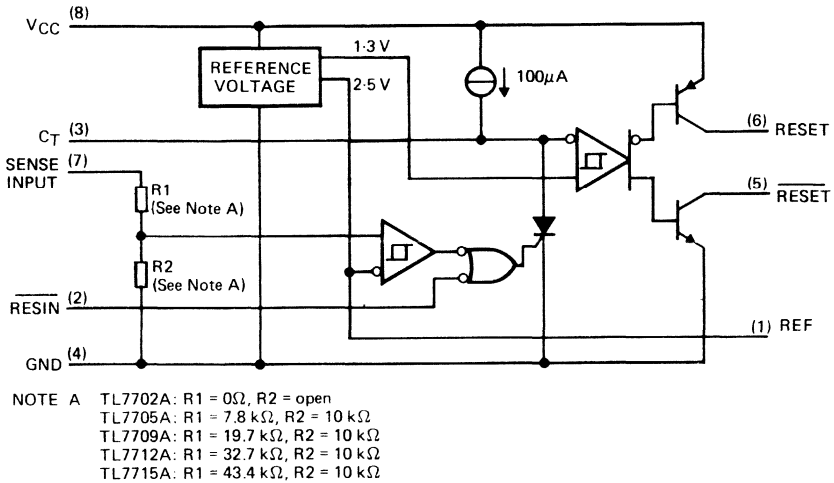
Fig. 7–2   Functional Diagram.

To achieve a high accuracy, this divider is adjusted at slice probe. When the input voltage is sensed to be lower than the threshold voltage, the thyristor is triggered, which discharges the timing capacitor C_T, It is also possible to fire the thyristor via the RESIN input by a logic level (TTL level, active LOW). The thyristor is turned off again when the voltage at the sense input increases beyond the threshold, (assuming RESIN input is above the threshold) or, during short supply voltage drops, the discharge current of the capacitor becomes lower than the hold current of the thyristor.

Thereafter, the capacitor is recharged by a current source 100 μA, the charge time being calculated as follows:

$$t_d = 1.3 \times 10^4 \times C_t \qquad C_t \text{ in F, t in sec}$$

An additional comparator compares the voltage at the capacitor with the reference voltage and forces the outputs into the active state as long as the voltage at the capacitor is lower than the reference voltage.
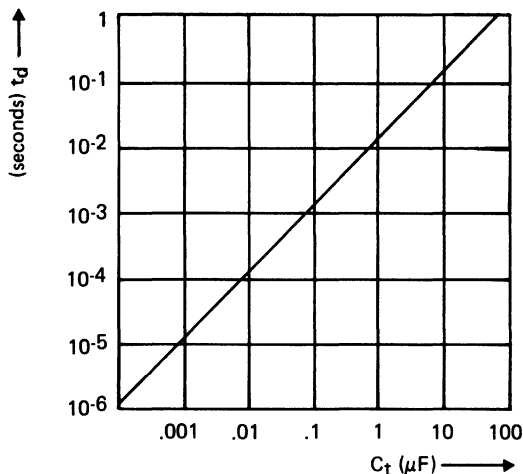
Fig. 7–3   Diagram for calculation of C_t.

Figure 7–4 shows the timing of the various signals. The SENSE input is connected to the supply voltage V_{CC} as in typical applications of this device. The minimum supply voltage for which the function of this device is guaranteed is 3 volts. Between POWER-ON and this voltage, the state of the outputs is not defined. In practical applications this is not a limitation because, at such supply voltages, the function of the RESET inputs of the other circuits is not guaranteed. Beyond this voltage the capacitor is first kept discharged, and the outputs stay in the active state. When the input voltage becomes higher than the threshold voltage V_s, the thyristor is turned off and the capacitor is charged. After a delay, t_d, the voltage passes the trigger level of the output comparator and the output becomes inactive. The microcomputer is therefore set to a defined initial state and starts the operation.

When the supply voltage falls below the minimum allowable value, the thyristor cuts in and the RESET process is thus introduced. Also the outputs remain in the active condition for the period t_d after the supply voltage returns. A hysteresis V_h in the input computing comparator prevents any oscillation of the input phase to be maintained during slow variations in the voltage.

The thyristor is triggered again during voltage drops below the minimum recommended value. The output stays in the active state for the time t_d after the return of the supply voltage to its required value.

The time t_d, and also the capacitor C_t, are determined by the requirements of the following circuitry. In TTL systems, theoretically, a RESET time of 20 to 50 ns is sufficient. For proper operation, microcomputers require a RESET signal which lasts for several machine cycles and is thus of the order of 10 to 200 µs, according to the type of microcomputer. In a practical application, the delay time will be determined by characteristics of the power supply. Care has to be taken that during and shortly after power-on, short voltage fluctuations do not repetitively reset the system. Delay times of 10 to 20 ms will usually avoid these problems.
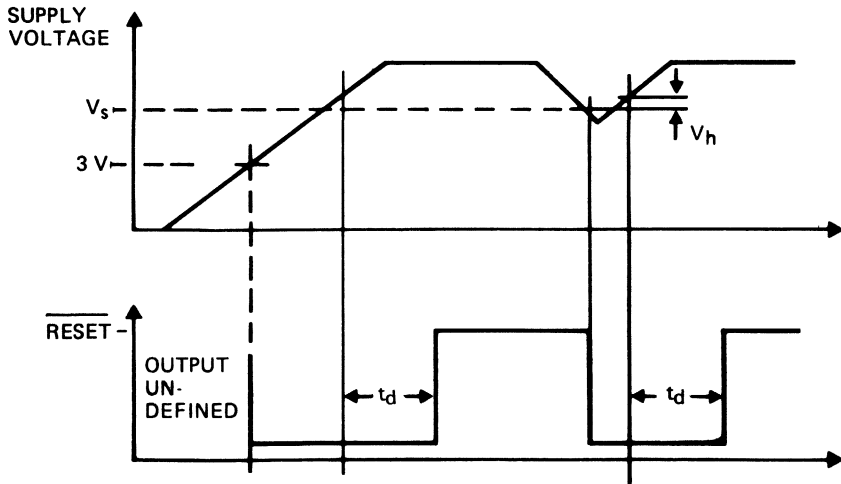
Note: SENSE Input connected to V_{CC}

Fig. 7–4   Timing diagram.

SUPPLY VOLTAGE SUPERVISOR APPLICATION EXAMPLES

Five versions of this circuit are available:

● TL7705A (V_T = 4.55 V): Application TTL systems and micro-computer systems which require a 5 volt supply.

● TL7709A (V_T = 7.6 V): Application in microcomputer systems using the TMS1XXNLL.

● TL7712A (V_T = 10.8 V): Application in CMOS, microp-rocessor, and memory circuits with a 12 volt supply.

● TL7715A (V_T = 13.5 V): Application in microcomputer systems using the TMS1XXXNLP.

● TL7702A (V_T = 2.53 V): Application in systems where other supply voltages are used. The required trigger level may be adjusted with an external resistor divider at the SENSE input.

Since for most applications, the circuits are already adjusted to the appropriate voltage levels, these devices are easy to use. Figure 7–5 and 7–6 show the circuit diagrams for a 5 volt and a 15 volt microcomputer system. The external components are the filter capacitor of the reference voltage and the timing capacitor C_t.
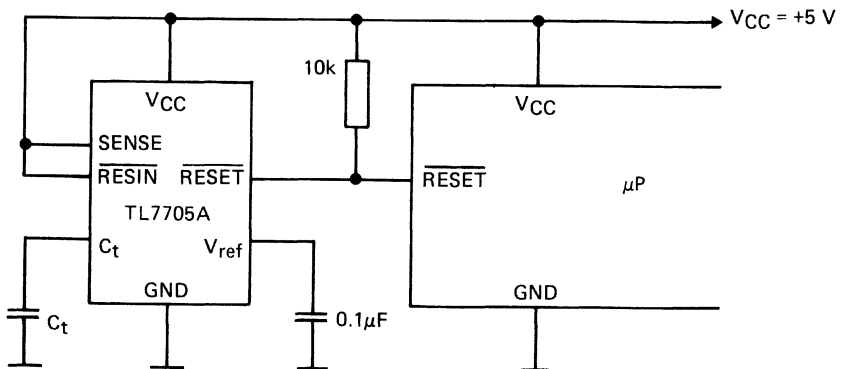
Fig 7–5. TL7705A in 5 volt microcomputer applications.
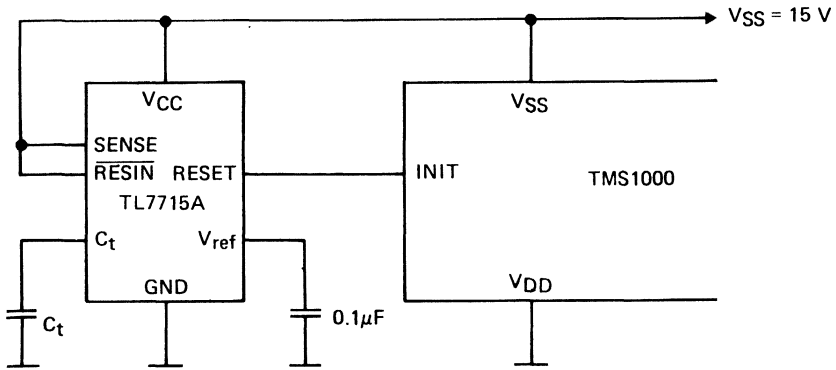
Fig. 7–6   TL7715A in TMS1XXNLP applications.

The outputs of this device do not have an integrated pull up (pull down) resistor. In Figure 7–5 a 10 kΩ pull up resistor is connected to the RESET input to ensure the proper HIGH level. In TMS1XXX applications this resistor is not required, because these microcomputers have an integrated pull down resistor at the INIT input.

In larger systems, where several supply voltages are required it is necessary to supervise all supply voltages which may cause dangerous conditions in case of power failure. In the circuit diagram of Figure 7–7, two TL7712A's are used to check the positive and negative 12 volt supplies. Their outputs are fed to the RESIN of the TL7705A, which supervises the 5 volt supply. The output of this device is a SYSTEM RESET signal, which becomes active whenever anyone of the three supply voltages fails.

The RESET Signal can be operated manually using a button which acts on the RESIN input of the positive 12 V TL7712A.

When designing this control system care should be taken that in the event of a positive or negative 12 V power failure there is a defined RESET Signal when there is still a 5 V supply. To achieve this the circuit which monitors the positive 12 V supply is fed by the 5 V supply. The RESET Signal of the circuit which monitors the negative 12 V supply is fed in via a voltage divider to the base of the BC546 Transistor which then controls the RESIN input of the TL7705A. The voltage divider is proportioned to make BC546 Transistor become active with a failure of the negative voltage.
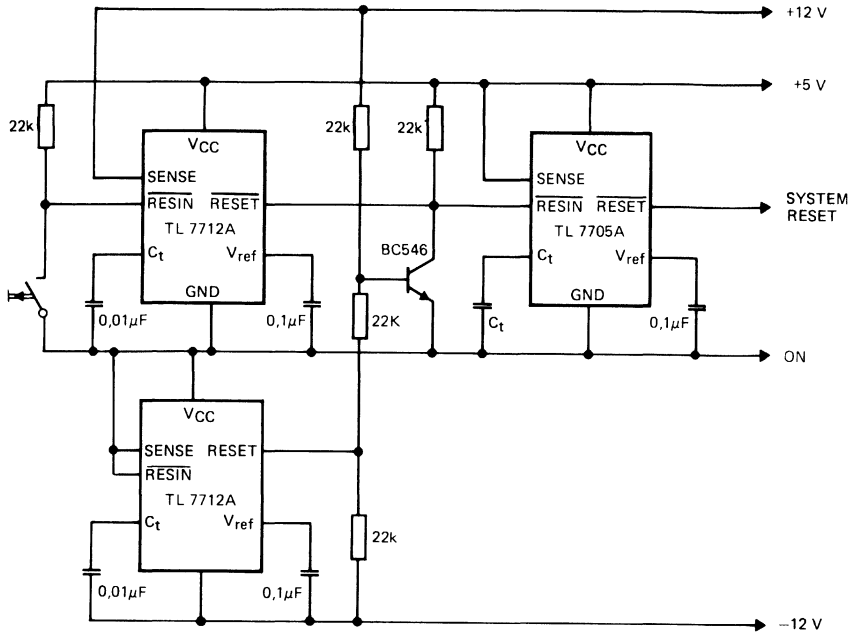
Fig. 7-7   Voltage supervision of a multiple power supply.

These supply voltage supervisor circuits were designed to detect very short voltage drops of 300 ns. In applications where this sensitivity is not required, the circuit may be delayed by adding a R/C network in front of the SENSE input (Figure 7–8). To avoid influence on threshold voltage of this input, the resistor should be less than 22 ohms. The
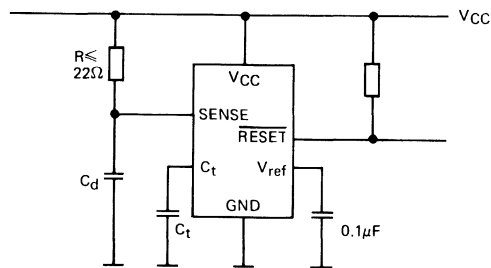
Fig. 7–8   Delayed triggering.

capacitor C_d is then calculated according to the required delay time $(t = C_d \times R)$.

In some applications it is necessary to keep the output of the reset circuit active when no supply voltage is applied. Under normal conditions the output transistor of the TL7700A is switched off (inactive state), when the supply voltage is lower than 3 V. In Figure 7–9 a P-channel field effect transistor is connected to the $\overline{\text{RESET}}$ output. This transistor conducts when the supply voltage drops below 3 V i.e. at a gate source voltage of −3 V or less. To ensure that the transistor is switched off when the supply voltage has reached the nominal value, the gate has to be at least 6 V more positive than the source (or the required HIGH level). In Figure 7–9 therefore the V_{CC} terminal of the TL7705A is connected to the filter capacitor in front of the voltage regulator.
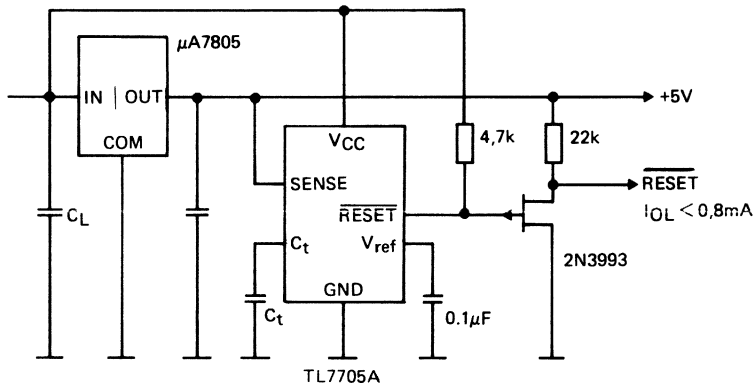
Fig. 7–9   Modified output circuit.

A further application for these integrated circuits is in battery-buffered memory systems. After failure of the line voltage, the content of the memory has to be protected against spikes on the write line. Generally, it is sufficient to switch the chip select line into the inactive state (some memories also require that the write line be disabled).

A switch, which consists of transistor T1 and diode D1, is inserted into the chip select line of the memory. Under normal operation (line voltage present) the output of the TL7705A is turned off (HIGH); the transistor T1 draws its base current from transistor T2 and resistor R1.

When the chip select line is switched from HIGH to LOW, the transistor conducts and the CS input of the memory goes LOW. Because of the small DC load of the resistor R2, the saturation voltage of the transistor (and therefore the shift of the LOW level at the CS input) is very small (typ. 40 mV). When the chip select line is switched HIGH again, the transistor T1 is turned off (the influence of the inverse current gain is negligible); the diode D1 conducts and charges the circuit capacitance. In case of a power-failure the TL7705A is triggered and its RESET output becomes LOW. The base of transistor T1 can no longer draw current. By this, the CS input of the memory is separated from the chip select line. In some cases it also recommended to disable the memory during the SYSTEM RESET via the RESIN input, to protect the content of the memory against spikes on the write line during this time.
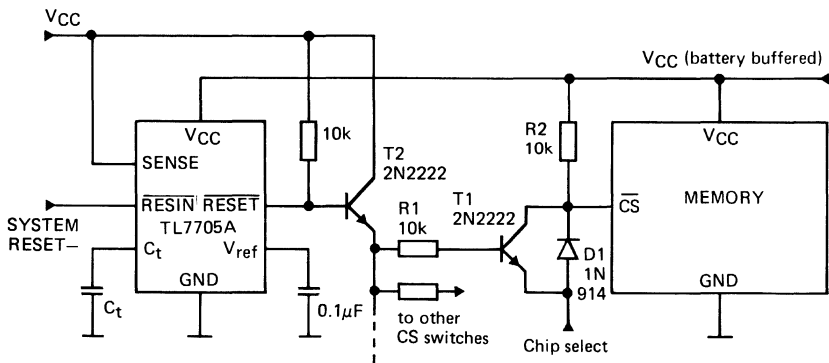
Fig. 7–10   Circuit diagram for memory protection.

OVERVOLTAGE SENSING CIRCUITS

The use of SCR crowbar overvoltage protection (OVP) circuits is a popular method for providing protection from accidental overvoltage stress for a power supply load. The sensing function for this type of OVP circuit can be provided by a single IC, the MC3423, as shown in Figure 7–11.
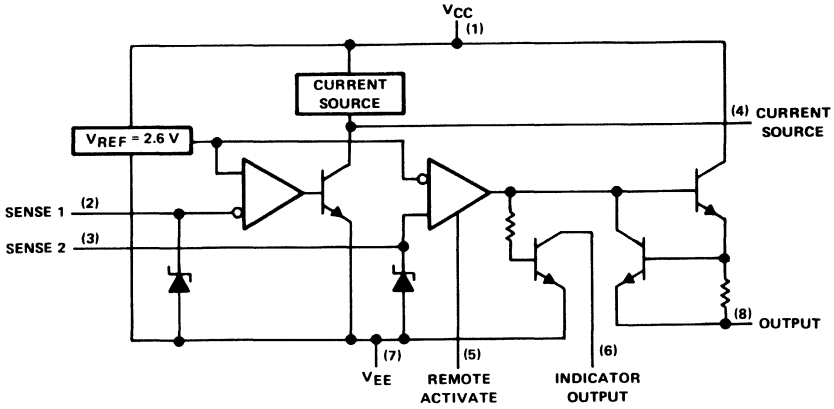
Fig. 7–11   MC3423 Overvoltage Crowbar Sensing Circuit Block Diagram.

The Crowbar Technique

One of the simplest and most effective methods of obtaining overvoltage protection is to use a crowbar SCR placed across the equipment's dc power supply bus. As the name implies, the SCR is used much like a crowbar would be, to short the input of the dc supply when an overvoltage condition is detected. A typical circuit configuration is shown in Figure 7–12.
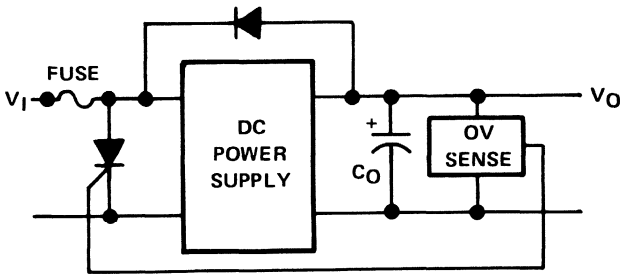
Fig. 7–12 Typical Crowbar Circuit.

The MC3423 operates from V_{CC} minimum of 4.5 V to a maximum of 40 V. The input error amplifier has a 2.6 V reference between the non-inverting input and V_{EE}. The inverting input is $V_{sense\ 1}$ (Pin 2) and is the point to which the output sense voltage is applied. This is usually

done through a resistor voltage divider which sets the trip point (V_{ref}) at 2.6 V. The output of the device. Pin 8, then triggers the gate drive terminal of the SCR. A basic OVP circuit is shown in Figure 7–13.
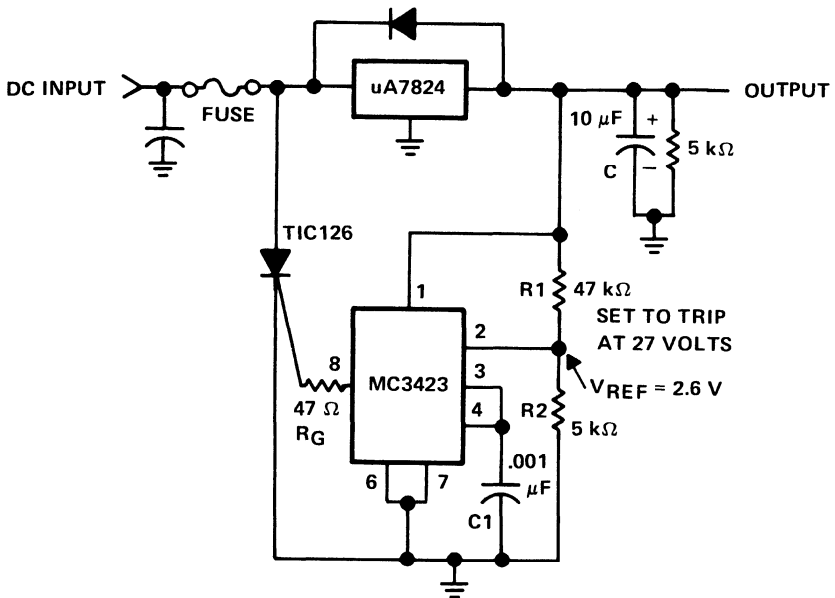
- **PROGRAMMABLE DELAY**
- **REMOTE ACTIVATION INPUT**
- **DELAYED TRIGGER**

$$V_{TRIP} = V_{REF}(1 + \frac{R1}{R2})$$

R2 ≤ 10 kΩ for minimum drift.

Fig. 7–13   Overvoltage Protection Circuit.

When V_{CC} rises above the trip point set by R1 and R2, an internal current source (Pin 4) begins charging capacitor C1 which is also connected to Pin 3. When triggered, Pin 8 supplies gate drive through the current limit resistor (R_G) to the gate of the SCR. The minimum value of R_G is given in Figure 7–14.

The value of capacitor C determines the minimum duration of the overvoltage condition necessary to trip the OVP. The value of C can be determined from Figure 7–15.

If the overvoltage condition disappears before C is charged, C discharges at a rate which is 10 times faster than the charging rate, and resets the timing feature until the next overvoltage condition occurs.
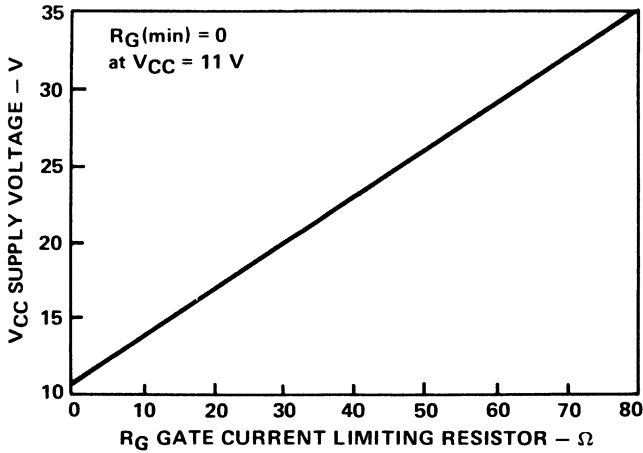
Fig. 7–14   Minimum R_G vs Supply Voltage.
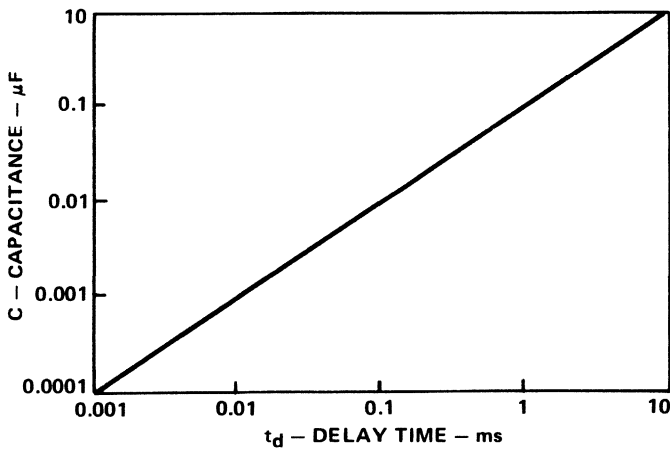
Fig. 7–15   Capacitance vs Minimum Overvoltage Duration.

Activation Indication Output

An additional output for use as an OV indicator is provided on the MC3423. This is an open-collector transistor which saturates when the OVP circuit is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC}, below 4.5 V.

This output may also be used to clock an edge-triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This method of protection reduces or eliminates the heat sinking requirements for the crowbar SCR.

Remote Activation Input

Another feature of the MC3423 is its remote activation input, Pin 5, which has an internal pull-up current source. This input is CMOS/TTL compatible and, when held below 0.8 V, the MC3423 operates normally. However, if it is raised above 2 V, the OVP is activated regardless of whether an overvoltage condition is present. This feature may be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition.

Section 8

Integrated Circuit Timers

Timing may be accomplished by a variety of methods; mechanical, thermal, chemical, or a combination of these. Regardless of the method, a timer depends upon a time base generated internally or applied from an external source. The spring-driven clock, for example, generates its own internal time base, whereas the electric clock uses the period of the ac line voltage as an external time base. The first consideration in the design of a solid state timer is the generation of a suitable time base.

RC TIME-BASE GENERATOR

A simple time base circuit may be established by the use of a resistor, a capacitor, and sensing network as shown in Figure 8–1.
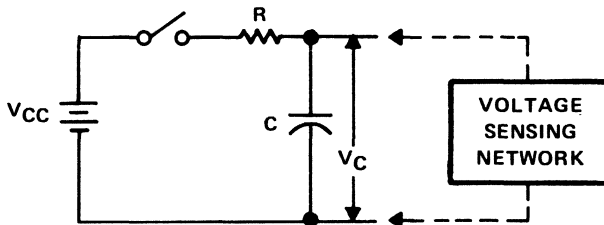
Fig. 8–1   Basic RC Circuit.

The time, t, for the capacitor C to charge to voltage V_C in this circuit is:

$$t = RC \ln \frac{V_{CC}}{V_{CC} - V_C}$$

where:

t = time in seconds

ln = natural log

R = resistance in ohms

C = capacitance in farads

V_C = capacitor voltage in volts

For one RC time constant (t = RC) V_C equals 63.21% of V_{CC}.

A BASIC DELAY TIMER

A basic delay circuit may be implemented with an RC network, a discharge switch, a voltage reference, a threshold comparator and an output switch. The timer circuit and its typical waveforms are illustrated in Figure 8–2.

(a) CIRCUIT

(b) VOLTAGE WAVEFORMS
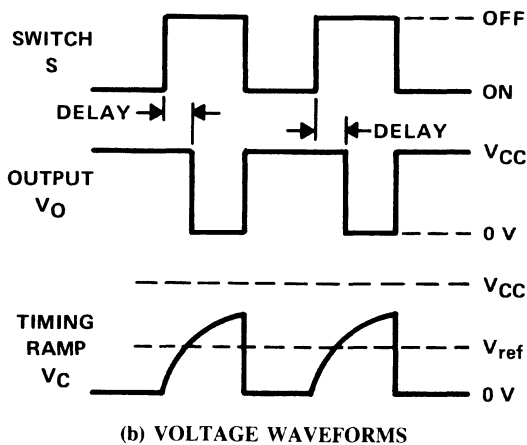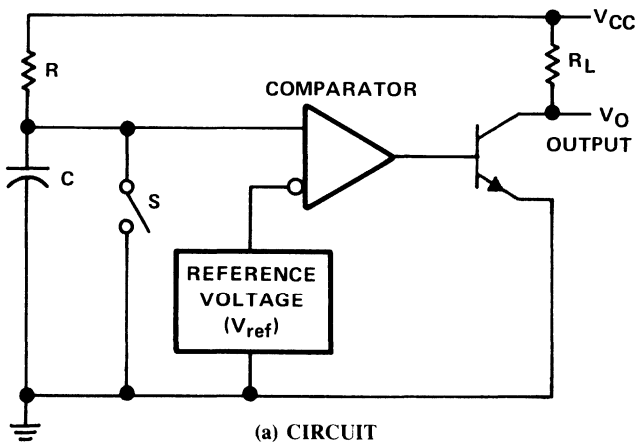
Fig. 8–2   Basic Delay Timer.

The circuit operates as follows: Initially the timer output (V_O) is high (near V_{CC}) and switch S is closed, shorting capacitor C to ground. When switch S is opened the timing period begins and V_O is still high.

When switch S is opened capacitor C starts charging, through resistor R, toward the V_{CC} rail. The voltage V_C rises non-linearly, forming a timing ramp (Figure 8–2(b)). V_O is delayed from changing state until V_C reaches the reference voltage, V_{ref}, which is some fraction of V_{CC}. When the timing ramp voltage reaches V_{ref} the comparator output goes high, turning on the output transistor, thus switching the output low. The output will remain low until the switch is closed or power is turned off.

The inclusion of another comparator, an RS type flip-flop and a discharge transistor to the structure shown in Figure 8–2 would allow a trigger pulse to start the timing function. In addition many other performance features including oscillation are possible. NE555 type IC timers have all of these functions, except the timing resistor and capacitor, included on a single chip.

NE/SE555 TIMERS

The NE555 was the first monolithic IC timer with multi-functional capabilities (introduced in 1972) and has been accepted as the standard for basic timing and oscillator functions. The NE555 (Figure 8–3) is a general-purpose bipolar IC capable of monostable and astable pulse generating modes covering a wide range of pulse durations and/or frequencies.

(a) FUNCTIONAL BLOCK DIAGRAM

(b) PINOUT PACKAGE
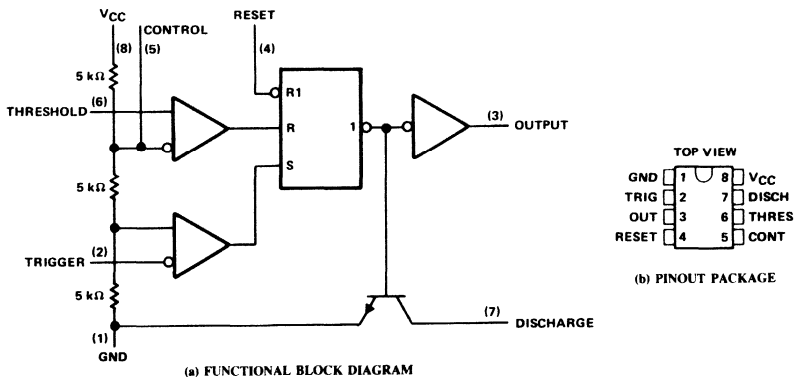
Fig. 8–3   NE555 Timer Block Diagram.

DEFINTION OF BLOCK DIAGRAM FUNCTIONS

Threshold Comparator

The threshold comparator compares its input with an internal reference level that is 2/3 V_{CC}. An input level greater than the reference will reset the timer's flip-flop resulting in a low output level and causing the discharge transistor to turn on. The internal reference is brought out on a pin allowing external control of the reference level to modify the timing period or reset the comparator. If this pin is not used it should be bypassed with a 0.01 μF capacitor to improve the timer's noise immunity.

Trigger Comparator

The trigger comparator compares its input with an internal reference level that is 1/3 V_{CC}. An input level less than 1/3 V_{CC} will set the flip-flop causing the output to go high and the discharge transistor to turn off. The trigger comparator functions on the leading (negative going) edge of the input pulse. Typically a minimum input pulse duration of 1.0 μs is required for reliable triggering. If the trigger input level remains lower than 1/3 V_{CC} for longer than one timing cycle, the timer will retrigger itself after the first output pulse. Propagation delay in the trigger comparator can delay turn off up to several microseconds after triggering. An output pulse duration of 10 μs or greater will prevent double triggering due to these effects.

RS Flip-Flop

The RS flip-flop receives its reset input from the threshold comparator, its set input from the trigger comparator and an additional reset from an external source. The external reset input overrides all other inputs and can be used to initiate a new timing cycle. When this input is at a logic low level the timer output is low and the discharge transistor is on, resulting in a reset condition. The reset input is TTL compatible. When not used it is recommended that the reset pin be connected to the V_{CC} rail to prevent false resetting.

Discharge Transistor

The discharge transistor will be on when the device output is low. Its open-collector output is used to discharge the external capacitor during the reset phase of operation.

Output Stage

The device output stage is driven by the flip-flop output. It is an active-pull-up, active-pull-down circuit with a 200 mA sink or source capability.

555 BASIC OPERATING MODES

There are two basic operating modes for 555 timer circuits: the monostable (one-shot) mode for timing functions, and the astable (free-running) mode for oscillator functions. There are many variations of the two basic models, allowing numerous applications.

Monostable Mode

Figure 8–4 illustrates the circuit and waveforms for the 555 connected on its most basic mode of operation – a triggered mono-stable.
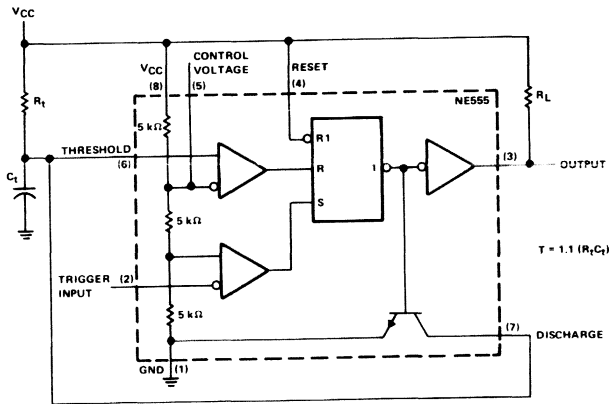
(a) CIRCUIT
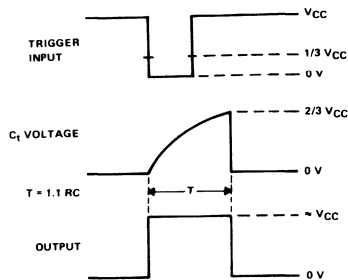
(b) VOLTAGE WAVEFORMS

Fig. 8–4   555 Triggered Monostable Circuit.

With the trigger input terminal held higher than $1/3$ V_{CC}, the timer is in its standby state and the output is low. When the trigger pulse appears with a level less than $1/3$ V_{CC}, the timer triggers and its timing cycle starts. The output switches to a high level near V_{CC} and concurrently C_t begins to charge toward V_{CC}. When the V_C voltage crosses $2/3$ V_{CC}, the timing period ends with the output falling to zero. The circuit is now ready for another input trigger pulse. The output pulse duration (T) is defined as $(1.1) \times R_t C_t$. In the monostable mode T is used to represent the on time which is the time base in this mode. With few restrictions, R_t and C_t can have a wide range of values. Assuming zero capacitor leakage current, there is no theoretical upper limit on T while the short pulse durations are limited by internal propagation delays to about 10 µs.

A reasonable lower limit for R_t, for 15 V operation is about 1 kΩ for the NE555 and is limited only by power dissipation considerations. The upper R_t limit, for V_{CC} of 15 V, is about 10 MΩ. Allowing for only 0.25 µA input leakage and 0.25 µA capacitor charging current the total current through R_t, at the threshold level would be 0.5 µA. R_t max is equal to the voltage across R_t at threshold, (which for a 15 V supply is 5 V), divided by 0.5 µA. This yields an R_t max of 10 MΩ. However, lower values should be used if accurate timing is required.

A practical minimum value for C_t is about 100 pF. Below this value stray capacitance becomes a limiting factor for timing accuracy. The maximum value for C_t is limited by capacitor leakage. Low leakage capacitors are available in values up to about 10 µF and are preferred for long timing periods. Capacitor values as high as 1000 µF could possibly be used if the leakage current is low enough for the application. The real limitation on C_t is leakage current and not capacitance. The ultimate criterion for the selection of R_t and C_t is the degree of accuracy desired. Staying within the limitations, illustrated in the 555 device data sheet charts, is recommended for relatively accurate designs.

As given in Figure 8–4(b), the pulse duration T is slightly more than an RC time constant (T = 1.1 RC). This is a result of a threshold level that is 66.7% of V_{CC} while one RC level is 63.2% of V_{CC}.

In a typical application input leakage currents may also lead to some slight differences between actual values of 'T' and calculated values. Operation at high speeds (very short pulse durations) will result in variations from the calculated values due to internal propagation delays.

Astable Mode

Figure 8–5(a) illustrates the 555 connected as an astable timer. Like the monostable circuit, the astable circuit requires only a few external components,
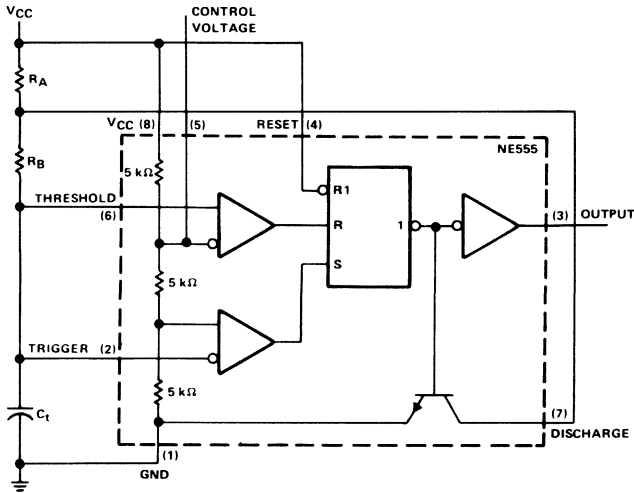
Fig. 8–5(a)   555 Astable Circuit.
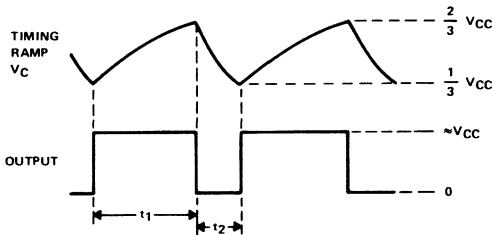
Fig. 8–5(b)   NE555 Astable Timing Diagram.

Figure 8–5(b) shows the timing diagram. The timing calculations are as follows.

$$t_1 = 0.693 \, (R_A + R_B) \, C_t$$

$$t_2 = 0.693 \, R_B C_t$$

$$T = 0.693 \, (R_A + 2R_B) \, C_t$$

where: t_1 is high-level output period

t_2 is low-level output period

T is total period $(t_1 + t_2)$

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C_t}$$

On startup, the voltage across C_t will be near zero which causes the timer to be triggered via pin 2. This forces the output high, turning off the discharge transistor and allows charging of C_t through R_A and R_B. C_t charges toward V_{CC} until its voltage reaches a level of 2/3 V_{CC}, at which point the upper threshold is reached, causing the output to go low and the discharge transistor to turn on. Capacitor C_t then discharges toward ground through R_B until its voltage reaches 1/3 V_{CC}, the lower trigger point. This retriggers the timer, beginning a new cycle. The timer threshold input therefore oscillates between the 2/3 V_{CC} and 1/3 V_{CC} comparator threshold levels.

The frequency of operation is simply the reciprocal of T as stated above. The duty cycle for either the high or low state is simply that period (t_1 or t_2) divided by the total period. For reliable operation, the upper frequency limit of the bipolar NE555 is about 100 kHz. Device upper frequency limitations are due to internal propagation delays. Low frequencies are not limited by the 555 devices but are limited by the leakage characteristics of C_t.

Specific duty cycles may be required in some applications. Duty cycle can be controlled (within limits) by adjusting the resistance of R_A and R_B in Figure 8–5(a). As R_B becomes large with respect to R_A, the duty cycle approaches 50% (square wave operation). Conversely, as R_A becomes large with respect to R_B, the duty cycle increases towards 100%. R_A must not be allowed to reach zero. Practical duty cycles range from 49.8% to 99% or in terms of resistor ratios R_A may be 1/100 of R_B or R_B may be 1/100 of R_A.

Accuracy

Although the 555 is a simple device, it performs accurately. In the monostable mode there is a typical initial error of only 1% due to process imperfections (R_t and C_t errors must be considered separately).

For astable operation the error is somewhat greater, typically about 2%. Drift with temperature is typically 55 ppm/°C (or 0.0055%/°C) for the monostable mode, and is about 150 ppm/°C for the astable mode.

TLC555 TIMER

In 1984, TI introduced a LinCMOS version of the 555 timer, the TLC555. It features the performance characteristics of a bipolar 555 and, in addition, some important improvements. Table 8–1 is a performance comparison of major parametric differences in the NE555 and TLC555.

Table 8–1   *Performance Comparison.*

SPECIFICATION	NE555	TLC555	UNITS
QUIESCENT CURRENT	6.0	0.3	mA
BIAS CURRENT	500,000	10	pA
MAXIMUM FREQUENCY	100	2000	kHz
CURRENT SPIKES	≥200	3	mA

Due to its high-impedance inputs, the TLC555 is capable of producing accurate time delays and oscillations using less expensive, smaller timing capacitors than the NE555. A duty cycle of 50% in the astable mode is easily achieved using only one resistor and one capacitor as illustrated in Figure 8–6.
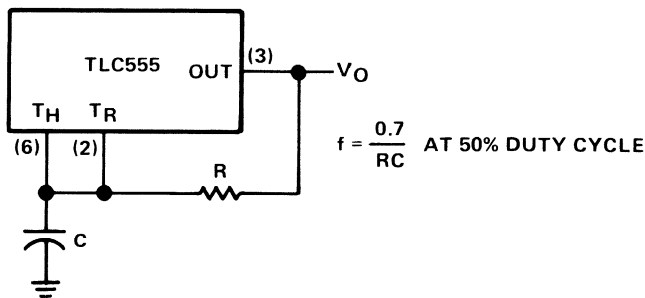
Fig. 8–6   TLC555 Astable Circuit.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC555 exhibits greatly reduced supply current spikes during output transitions (see Table 8–1). This minimizes the need for the large decoupling capacitors required by the bipolar 555.

The TLC555 also provides very low power consumption (typically 1 mW at V_{DD} = 5 V) for supply voltages ranging from 2 V to 18 V.

TLC555 Astable Timing Equations

At astable operating frequencies above one megahertz, the propagation delays of the TLC555 must be accounted for in the equations for calculating the astable frequency (see Figure 8–7). The on-state resistance (R_{Don}) of the NMOS discharge transistor (typically 10 Ω) is also included to give greater accuracy. Besides the low to high and high to low propagation delays, (t_{PLH} and t_{PHL} respectively), two additional times, T_C and T_D, must also be included along with the maximum charge and minimum discharge voltages, (V_h and V_l respectively).

As the capacitor is charging, it continues to charge up to V_h after crossing the 2/3 V_{DD} level for a time equal to the t_{PHL} propagation delay. T_D is the length of time it takes to discharge from V_h to 2/3 V_{DD}.
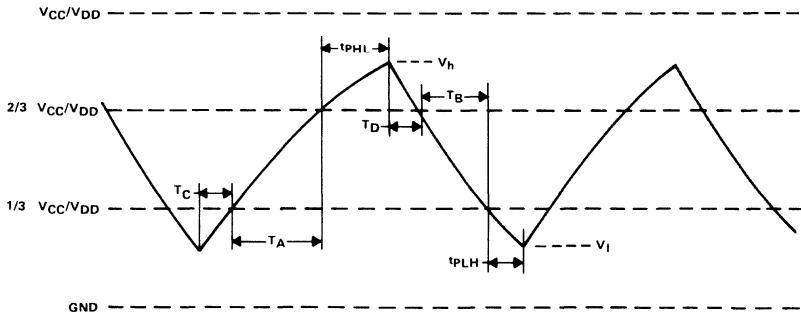
Fig. 8–7   TLC555 Astable Timing Diagram.

Likewise, during the discharge part of the cycle the capacitor continues to discharge to V_l after crossing the 1/3 V_{DD} level for a time equal to t_{PLH}. T_C is the length of time required to charge back up from V_l to 1/3 V_{DD}.

$$R_T = R_A + R_B$$

$$R_T' = R_B + R_{Don}$$

$$T_A = 0.693\ R_T C_t$$

$$\therefore V_h = (2/3)V_{DD}\{1 - EXP[- (0.693 + t_{pHL}/R_TC_T)]\} + (1/3)V_{DD}$$

$$\therefore V_1 = (2/3)V_{DD} \, EXP[- (0.693 + t_{pLH}/R_T'C_T)]$$

$$\therefore T_C = - R_tC_t \ln\{1 - [(1/3)V_{DD} - V_1]/(V_{DD} - V_1)\}$$

$$\therefore T_D = (- R_T'C_t) \ln [(2/3)V_{DD}/V_h]$$

$$\therefore T_{period} = T_A + T_B + T_C + T_D + t_{PLH} + t_{PHL}$$

$$\therefore f_{astable} = 1/T_{period}$$

Notice that for t_{PLH}, t_{PHL}, and R_{Don} equal to zero the above equations reduce to the standard equation as printed in the data book for the NE555:

$$(NE555) \; T_{period} = T_A + T_B = 0.693(R_A + 2R_B) \, C_t$$

It should also be noted that a 10% increase in astable frequency will also occur if a 0.1 μF capacitor is connected from the control voltage pin (pin 5) to ground.

TLC556/NE556 DUAL UNIT

The NE556 bipolar timer contains two NE555 timers in the same package, with common power-supply and ground pins. The LinCMOS version of the dual 555 timer is the TLC556. See Figure 8–8 for the pinout of these devices.

(TOP VIEW)

```
          ┌─────────┐
   DSCH  ─┤1  ∪  14├─  V_DD
  THRES  ─┤2     13├─  DSCH
   CONT  ─┤3     12├─  THRES
  RESET  ─┤4     11├─  CONT
    OUT  ─┤5     10├─  RESET
   TRIG  ─┤6      9├─  OUT
    GND  ─┤7      8├─  TRIG
          └─────────┘
```

TIMER #1 (pins 1–7), TIMER #2 (pins 8–14)
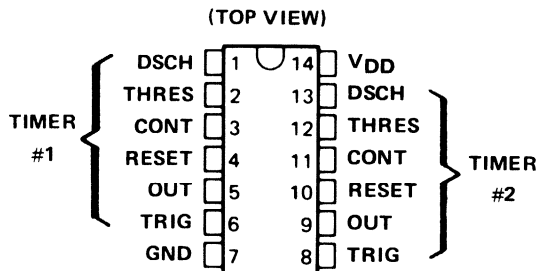
Fig. 8–8   Dual Timer Pinout.

The TLC556 dual timer is identical to the NE556 electrically and functionally. It is fabricated using the LinCMOS process and has the same advantages noted for the TLC555.

'555' APPLICATION CIRCUITS

Missing Pulse Detector

Figure 8–9 illustrates an NE555 timer utilized as a missing pulse detector. This circuit will detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timer is connected in the monostable mode. In addition, a 2N2907 is connected with the collector grounded and the emitter tied to pins 6 and 7. This outboard switch is in parallel with the internal discharge transistor. The transistor base is connected to the trigger input of the NE555.
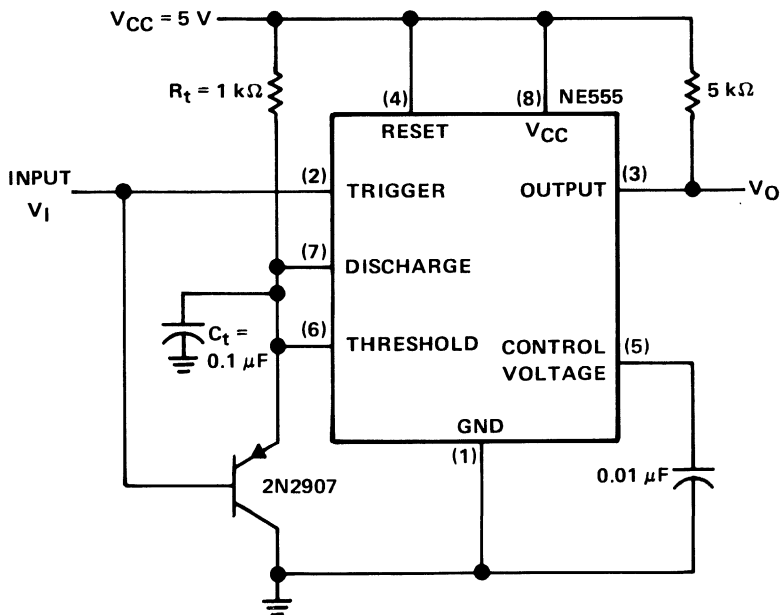
Fig. 8–9   Missing Pulse Detector Circuit.

For this application, the time delay should be set slightly longer than the timing of the input pulses. The timing interval of the monostable circuit is continuously retriggered by the input pulse train (V_I). The pulse spacing is less than the timing interval, which prevents V_C from rising high enough to end the timing cycle. A longer pulse spacing, a missing pulse, or a terminated pulse train will permit the timing interval to be completed. This will generate an output pulse (V_O) as illustrated in Figure 8–10. the output remains high on pin 3 until a missing pulse is detected at which time the output goes low.
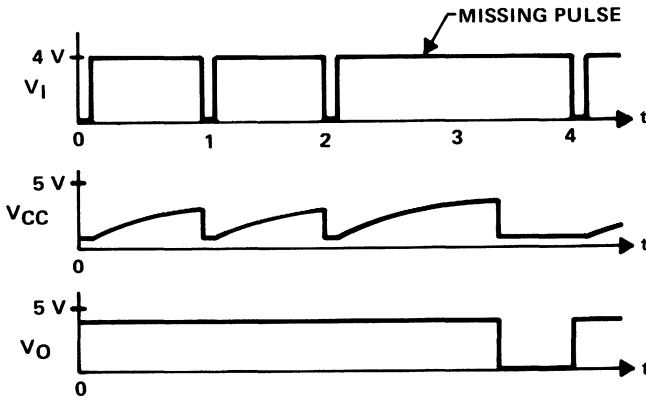
Fig. 8–10   Missing Pulse Detector Waveforms.

The input cannot be more than twice this free-running frequency or it would retrigger before the timeout and the output would remain in the low state continuously. The example in Figure 8–9 operates in the monostable mode at about 8 kHz so pulse trains of 8 to 16 kHz may be observed.
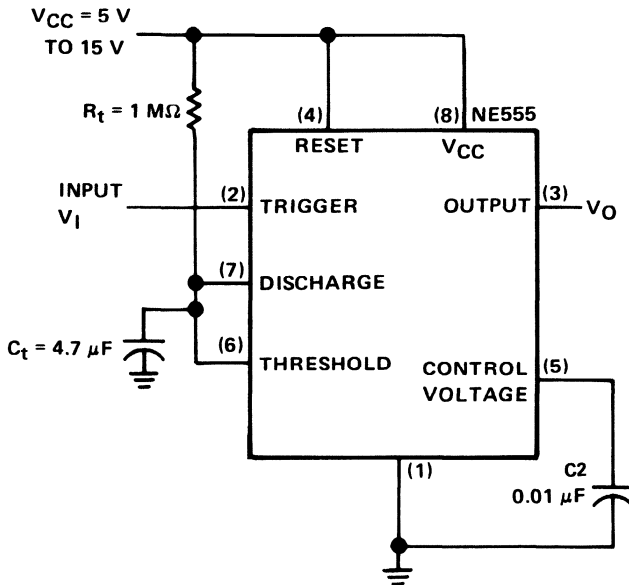
Fig. 8–11   NE555 One-Shot Timer.

NE 555 One-Shot Timer

Figure 8–11 shows the NE555 connected in its most basic mode of operation, a triggered monostable one-shot, the operation of which has been described previously. This simple circuit consists of only the two timing components R_t and C_t, the NE555, and bypass capacitor C2. While not essential for operation, C2 is recommended for noise immunity.

Due to the internal latching mechanism, the timer will always time out when triggered, regardless of any subsequent noise (such as bounce) on the trigger input. For this reason the circuit can also be used as a bounceless switch by using a shorter RC time constant. A 100 KΩ resistor for R_t and a 1 μF capacitor for C_t would give a clean 0.1 s output pulse when used as a bounceless switch.

Oscilloscope Calibrator

The circuit shown in Figure 8–12 can be used to check the accuracy of an oscilloscope time-base generator as well as to calibrate the input level of the amplifiers.
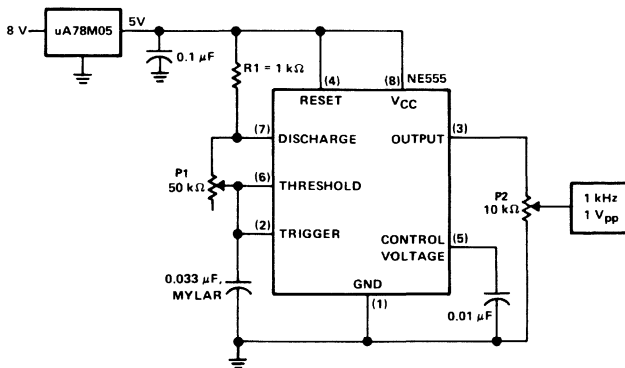
Fig. 8–12   Oscilloscope Calibrator.

The calibrator consists of an NE555 connected in the astable mode. The oscillator is set to exactly 1 kHz by adjusting potentiometer P1 while the output at pin 3 is being monitored against a known frequency

standard or frequency counter. The output level likewise is monitored from potentiometer P2's centre arm to ground with a standard instrument. P2 is adjusted for 1 V peak-to-peak at the calibrator output terminal. The circuit may be supplied with at least 8 V and is regulated to 5 V to supply the NE555.

During operation, the calibrator output terminal will produce a 1 kHz square wave signal at 1 V peak-to-peak with about 50% duty cycle. For long term oscillator frequency stability, C1 should be a low leakage mylar capacitor.

Darkroom Enlarger Timer

An enlarger timer is essential for consistent quality and repeatability. The timer controls the exposure time of the paper in the enlarger.
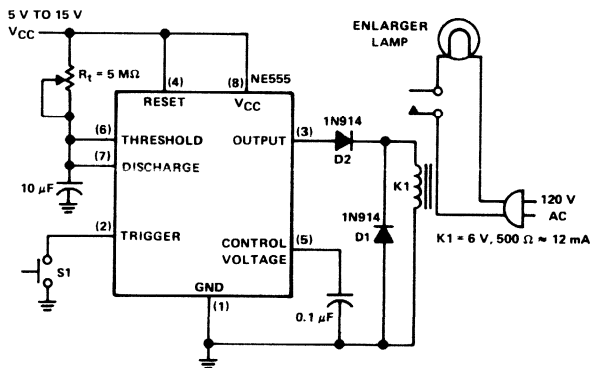
Fig. 8–13   Darkroom Enlarger Timer.

The NE555 circuit illustrated in Figure 8–13 is a basic one-shot timer with a relay connected between the output and ground. It is triggered with the normally open momentary contact switch which when operated, grounds the trigger input (pin 2). This causes a high output to energize K1 which closes the normally open contact in the lamp circuit. It remains closed during the timing interval and opens at time out. Timing is controlled by a 5 MΩ potentiometer, R_t. All timer driven relay circuits should use a reverse clamping diode, such as D1, across the coil. The purpose of diode D2 is to prevent a timer output latch up condition in the presence of reverse spikes across the relay.

With the RC time constant shown, the full scale time is slightly less than one minute. A scale for shaft position of the 5 MΩ potentiometer can be made and calibrated in seconds. Longer or shorter full scale times may be achieved by changing the values of the RC timing components.

Touch Switch

An interesting type of circuit that uses an IC timer is shown in Figure 8–14. This circuit is a 'touch switch', a device in which switching action is accomplished without conventional mechanical movement of a lever or push button. A circuit such as this could be used in a burglar alarm.
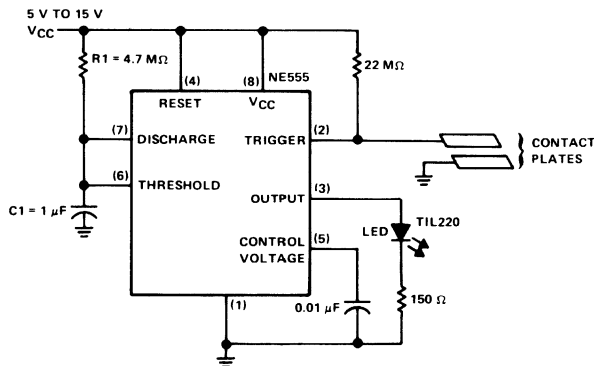
Fig. 8–14   Touch Switch.

The circuit is basically an NE555 monostable, the only major difference being its method of triggering. The trigger input is biased to a high value by the 22 MΩ resistor. When the contact plates are touched, the skin resistance of the operator will lower the overall impedance from pin 2 to ground. This action will reduce the voltage at the trigger input to below the 1/3 V_{CC} trigger threshold and the timer will start. The output pulse width will be T = 1.1 R1C1, in this circuit about 5 seconds. A relay connected from pin 3 to ground instead of the LED and resistor could be used to perform a switching function. Similarly to the circuit shown in Figure 8–13, diodes should be used in conjuction with the relay.

The contact strips or plates may be copper, brass, or any conducting material arranged for convenient finger contact.

Basic Square Wave Oscillator

A basic square wave oscillator is shown in Figure 8–15 and is useful in test equipment applications requiring a signal generator for testing other circuits. The NE555 is connected in the astable mode and uses only three timing components (R_A, R_B, and C_t). A 0.01 μF bypass capacitor is used on pin 5 for noise immunity.

Operating restrictions of the astable mode are few. The upper frequency limit is about 100 kHz for reliable operation, due to internal storage times. Theoretically there is no lower frequency limit, only that imposed by R_t and C_t limitations. There are many variations of this astable circuit, but it is shown here in its simplest form.

Oscillators such as this are useful in test equipment or as a signal generator for testing other circuits.
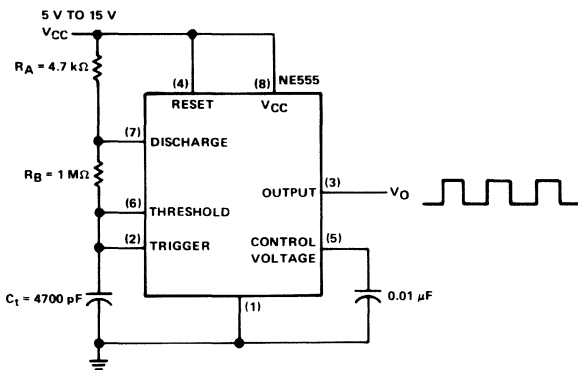
Fig. 8–15   Basic Square Wave Oscillator.

The frequency for the circuit in Figure 8–15 may be calculated as follows.

$$f = \frac{1.44}{(R_A + 2R_B)C_t}$$

$$= \frac{1.44}{(4.7K + 2M)(0.0047\ \mu F)}$$

$$= \frac{1.44}{9.42209 \times 10^{-3}}$$

$$f = 152.8\ Hz$$

Linear Ramp Generator

A very useful modification to the standard monostable configuration is to make the timing ramp a linear waveform, rather than an exponential one. The linear charging ramp is most useful where linear control of voltage is required. Some possible applications are a long period voltage controlled timer, a voltage to pulse width converter, or a linear pulse width modulator.
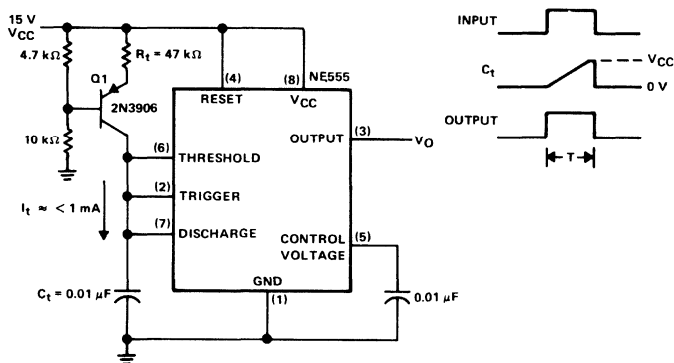
Fig. 8–16   Linear Ramp Generator.

One of the simplest methods to achieve a linear ramp monostable is to replace the timing resistor, R_t, with a constant current source as illustrated in Figure 8–16. Q1 is the current source transistor, supplying constant current to the timing capacitor C_t. When the timer is triggered, the clamp on C_t is removed and C_t charges linearly toward V_{CC} by virtue of the constant current supplied by Q1. The threshold at pin 6 is 2/3 V_{CC} here, it is termed V_C. When the voltage across C_t reaches V_C volts, the timing cycle ends. The timing expression for output pulse width T is:

$$T = \frac{V_C C_t}{I_t}$$

where: V_C is the voltage at pin 6
        I_t is the current supplied by Q1

I_t can be approximated for $V_{CC} = 15$ V as:

$$I_t = \frac{4.2 \text{ V}}{R_t} \approx \frac{1}{0.24 \text{ R}_t}$$

Then T is: $T \approx 0.24 \text{ V}_C R_t C_t$

$$\approx 0.24 \,(10)(47 \text{ k}\Omega)(0.01 \text{ }\mu\text{F})$$

$$\approx 1 \text{ ms}$$

The ramp frequency f_o is then:

$$f_o = \frac{1}{2T} = \frac{1}{0.002} = 0.5 \text{ Hz}$$

In general, I_t should be 1 mA or less, and C_t can be any value compatible with the NE555.

Fixed-Frequency Variable-Duty-Cycle Oscillator

In a basic astable timer configuration timing periods t_1 and t_2, as shown in Figure 8–17, are not controlled independently. This makes it difficult to maintain a constant period (T) if either t_1 or t_2 is varied.
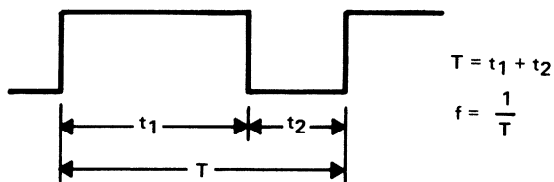
Fig. 8–17   Astable Mode Output Timing.

A number of methods have been developed to maintain a constant period T for this versatile timer. One method, as illustrated in 8–18, employs a circuit that adds two diodes to the circuit.
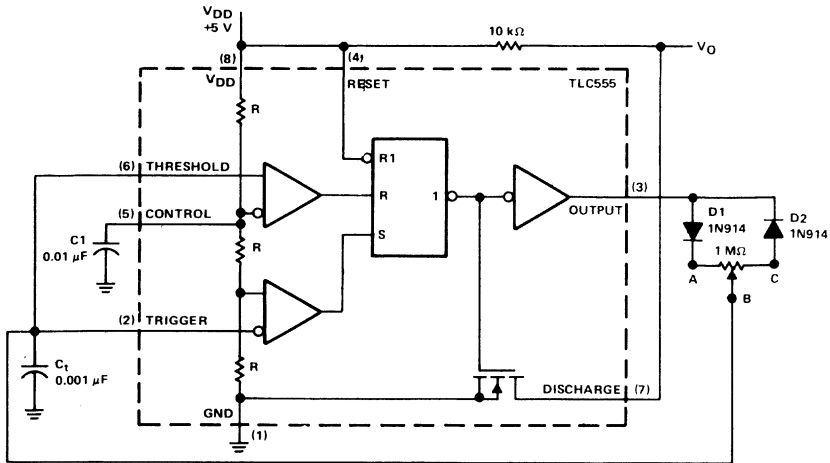
Fig. 8-18   Fixed-Frequency Variable-Duty Cycle Astable Oscillator.

In this circuit the charge (R_{AB}) and discharge (R_{BC}) resistances are determined by the position of the common wiper arm (B) of the potentiometer making it possible to adjust the duty-cycle by adjusting t_1 and t_2 proportionately without changing the period T.

At startup, the voltage across C_t is less than the trigger level voltage (1/3 V_{DD}), causing the timer to be triggered via pin 2. The output of the timer (pin 3) goes high, turning off the discharge transistor (pin 7) and allowing C_t to charge through diode D1 and resistance R_{AB}.

When capacitor C_t charges to the upper threshold voltage (2/3 V_{DD}), the flip-flop is reset and the output (pin 3) goes low. Capacitor C_t then discharges through diode D2, via resistance R_{BC}. When the voltage at pin 2 reaches 1/3 V_{DD}, the lower threshold or trigger level, the timer triggers again and the cycle is repeated.

In this circuit the oscillator frequency remains fixed and the duty cycle is adjustable from <0.5% to >99.5%.

Alternating LED Flasher

Alternating LED action is easily accomplished using the circuit shown in Figure 8-19 with the TLC555 operating in the astable mode.
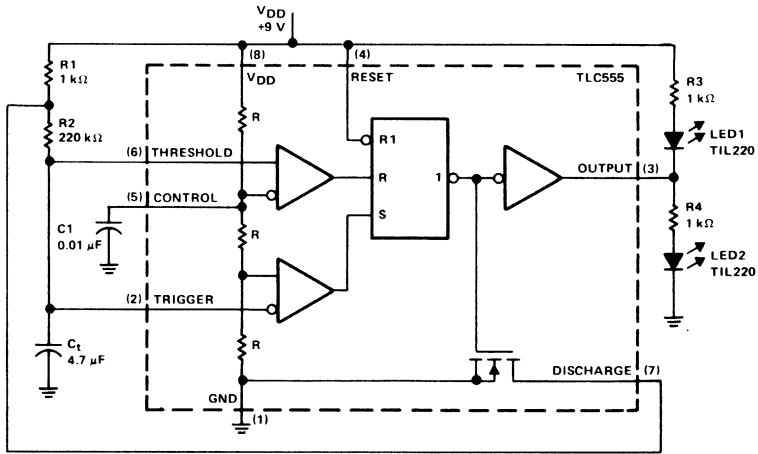
Fig. 8–19   Alternating LED Flasher.

The timing components are R1, R2, and C_t. C1 is a bypass capacitor used to reduce the effects of noise. At startup, the voltage across C_t is less than the trigger level voltage (1/3 VDD), causing the timer to be triggered via pin 2. The output of the timer (pin 3) goes high, turning LED1 off, LED2 on, the dischage transistor (pin 7) off, and allowing C_t to charge through resistors R1 and R2.

When capacitor C_t charges to the upper threshold voltage (2/3 V_{DD}), the flip-flop is reset and the output (pin 3) goes low. LED1 is turned on, LED2 is turned off, and capacitor C_t discharges through resistor R2 and the discharge transistor. When the voltage at pin 2 reaches 1/3 V_{DD}, the lower threshold or trigger level, the timer triggers again and the cycle is repeated.

The totem-pole output at pin 3 is a square wave with a duty cycle of about 50%. The output alternately turns on each LED at slightly less than one blink per second.

If the unit is battery operated, the TLC555 uses minimum current to produce this function. With a 9 V battery the circuit draws 5 mA (no load) and 15 mA when turning on an LED. Most of the ON current is LED current.

Voltage-Controlled Oscillator

There are many different types of voltage controlled oscillator (VCO) circuits that can use an IC timer. VCO circuits are valuable for instrumentation, electronic music applications, and function generators. The output is a rectangular pulse stream whose frequency is related to the external control voltage. A VCO circuit using the TLC555 is shown in Figure 8–20.
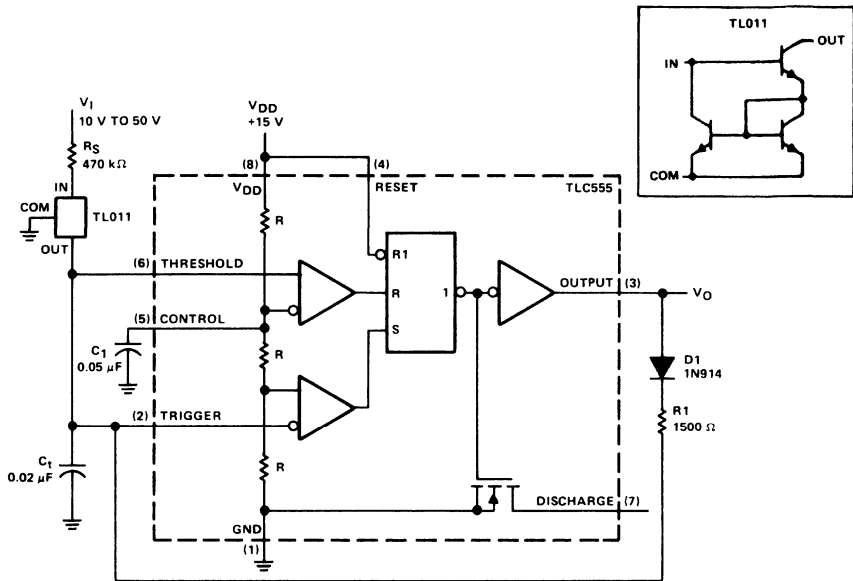
Fig. 8–20   Voltage-Controlled Oscillator.

At startup, the voltage at the trigger input (pin 2) is less than the trigger level voltage (1/3 V_{DD}), causing the timer to be triggered via pin 2. The output of the timer (pin 3) goes high, allowing capacitor C_t to charge very rapidly through diode D1 and resistor R1. The charge time of C_t is extremely short and may essentially be neglected.

When capacitor C_t charges to the upper threshold voltage (2/3 V_{DD}) the flip-flop is reset, the output (pin3) goes low, and capacitor C_t dischages through the npn current mirror, TL011. When the voltage at pin 2 reaches 1/3 V_{DD}, the lower threshold or trigger level, the timer triggers again and the cycle is repeated.

The input voltage (V_I) determines the constant current of the current mirror, which is used as a voltage to current converter and sets the discharge rate of capacitor C_t. The discharge time of C_t determines the frequency of the oscillator. As the input voltage is varied from 10 V to 50 V, the output frequency varies at a linear rate.

As an example, assume an application calls for an output midrange frequency of 500 Hz. Since T = 1/f, the time between output pulses will be 2 ms. The charge time, which will be less than 1 μs, may be neglected. The discharge current of C_t for a specific input control voltage is:

$$I_{DISCHARGE} = \frac{V_I}{R_S} = \frac{10\ V}{470\ k\Omega} = 20\ \mu A \text{ at 10 V input}$$

$$I_{DISCHARGE} \text{ at midrange} = 50\ \mu A \text{ at 25 V input}$$

$$I_{DISCHARGE} = \frac{V_I}{R_S} = \frac{50\ V}{470\ k\Omega} = 100\ \mu A \text{ at 50 V input}$$

With an input voltage of 10 V to 50 V, the TL011 current will vary linearly from 20 μA to 100 μA. Figure 8–21 shows the voltage to frequency conversion obtained with two different values for capacitor C_t. With C_t = 0.001 μF, a frequency range of 3.3 kHz to 10 kHz is obtained. When a value of 0.02 μF is used, a frequency range of 187 Hz to 1 kHz is obtained.
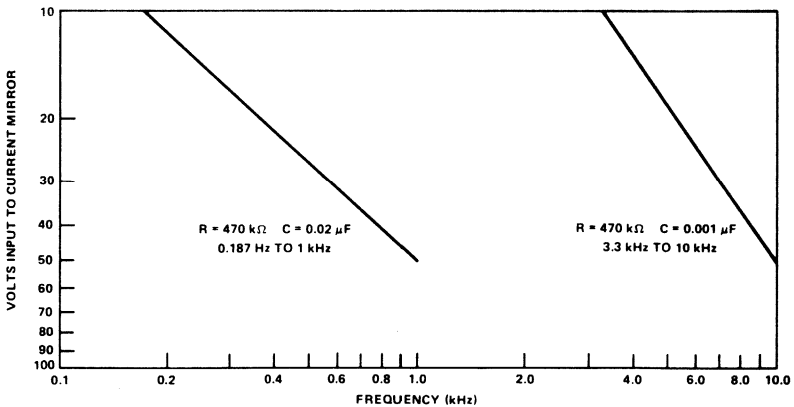
Fig. 8–21   Voltage-Controlled Oscillator Frequency vs Voltage.

Since the capacitor, C_t, discharges from 10 V to 5 V (2/3 V_{DD} to 1/3 V_{DD}), the capacitor value may be calculated for 500 Hz as follows:

$$C = \frac{IT}{V_C} = \frac{(50\ \mu A)\ (0.002)}{5}$$

I = midrange discharge current

$$T = \frac{1}{f} = \text{midrange output pulse}$$

V_C = 5 V (charge-discharge)

$$C = \frac{(50 \times 10^{-6})\ (0.002)}{5} = 0.02\ \mu F$$

Note that the current mirror is sinking current during both the charge and discharge of C_t. However, the small discharge current is easily overcome during the charge cycle by the lower impedance, high-current charge path from the output pin.

For linear ramp applications, the output is obtained across C_t.

Capacitance-to-Voltage Meter

The circuit can be more easily analyzed by examining the individual sections as shown in Figure 8–22.

Fig. 8–22   Capacitance-to-Voltage Meter Chart.

Timer U1 operates as a free-running oscillator at 60 Hz, providing trigger pulses to timer U2 which operates in the monostable mode. Resistor R1 is fixed and capacitor Cx is the capacitor being measured. While the output of U2 is 60 Hz, the duty cycle depends on the value of Cx. U3 is a combination low-pass filter and unity-gain follower whose dc voltage output is the time-averaged amplitude of the output pulses of U2, as shown in Figure 8–23 (a and b).
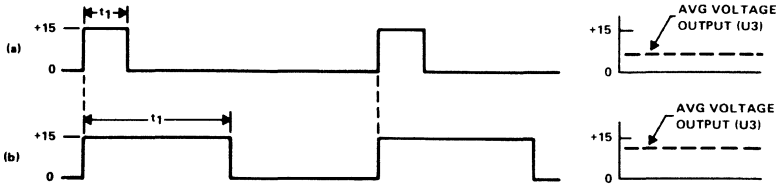
Fig. 8–23   U2 Duty Cycle Change.

Figure 8–23(a) shows when the value of Cx is small the duty cycle is relatively low. The output pulses are narrow and produce a lower average dc voltage level at the output of U3. As the capacitance value of Cx increases, the duty cycle increases making the output pulses at U2 wider and the average dc level output at U3 increases.
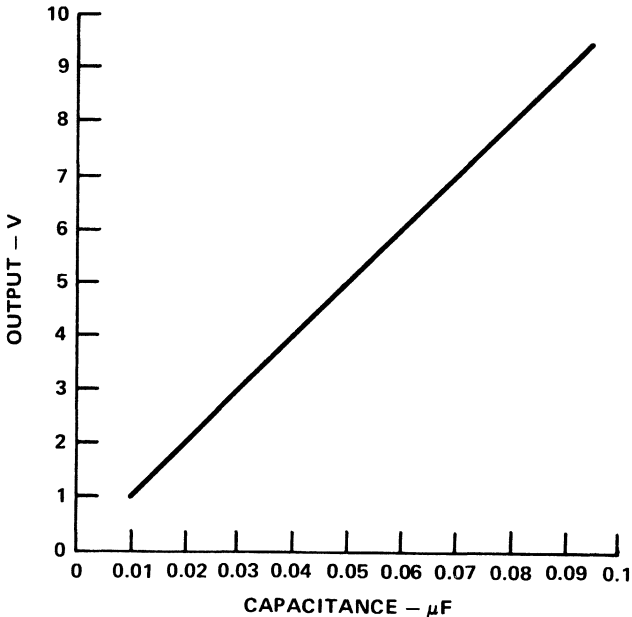
Fig. 8–24   Capacitance-to-Voltage Converter.

As an example, the graph in Figure 8–24 illustrates capacitance values of 0.01 µF to 0.1 µF plotted against the output voltage of U_3. Notice the excellent linearity and direct one-to-one scale calibration of the meter. If this does not occur with your design, the 100 kΩ resistor, R1, can be replaced with a potentiometer which can be adjusted to the proper value for the meter being used.

TLC555 PWM Motor Controller

The speed of a dc motor is proportional to the applied voltage, but the torque diminishes at low voltages. Low speed performance is usually erratic when analog controllers are used, especially under changing load conditions. Pulse-width-modulated (PWM) controllers offer superior control and operate efficiently at low speeds.
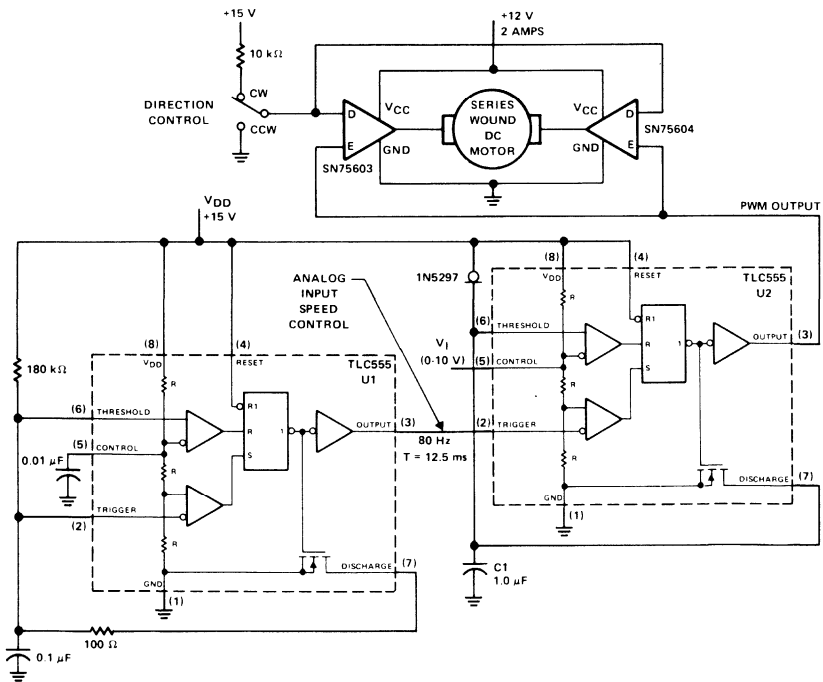
Fig. 8–25   TLC555 PWM Motor Controller.

The PWM controller shown in Figure 8–25 uses complementary half-H peripheral drivers (SN75603, SN75604) with totem-pole outputs rated at 40 V and 2.0 A. These drivers effectively place the motor in a full bridge configuration which has the ability to provide bidirectional control.

Timer U1 operates in the astable mode at a frequency of 80 Hz. The 100 Ω discharge resistor results in an 8 μs trigger pulse which is coupled to the trigger input of timer U2. Timer U2 serves as the PWM generator. Capacitor C1 is charged linearly with a constant current of 1 mA from the 1N5297, which is a FET current regulator diode.

Motor speed is controlled by feeding a dc voltage of 0 to 10 V to the control input (pin 5) of U2. As the control voltage increases, the width of the output pulse (pin 3) also increases. These pulses control the on/off time of the two motor drivers. Note that the trigger pulse width of timer U1 limits the minimum possible duty cycle from U2. Figure 8–26 illustrates the analog control voltage versus drive motor pulse width.
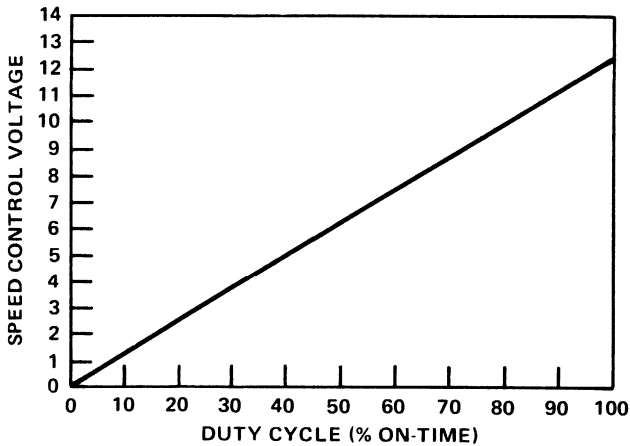
Fig. 8–26   Control Voltage Versus Duty Cycle.

Figure 8–27 illustrates the output waveforms of U1 with respect to the output of U2. The maximum duty cycle that may be achieved is about 98% at which time the control is 12.5 V.
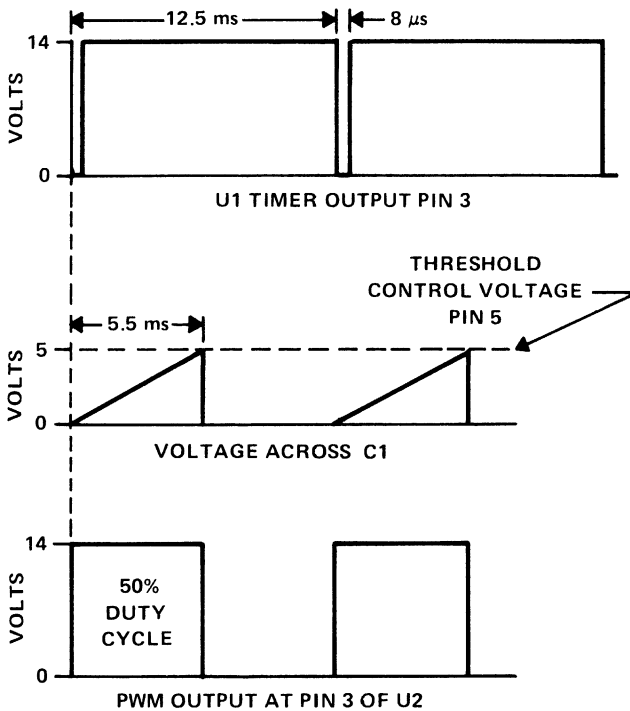
Fig. 8–27   PWM Controller Waveforms.

CAUTION: Careful grounding is required to prevent motor-induced noise interfering with the proper operation of the U1 and U2 timer circuits. Supply lines must be bypassed and decoupled at each timer to prevent transients from causing circuit instability. Separate power supplies should be used for the motor and the timer circuits.

Telephone Controlled Night Light

This application is a useful addition for the bedroom telephone stand. When the telephone rings, or when the handset is lifted, the night

light is turned on and remains on while the conversation takes place. When the handset is replaced in the cradle, the light remains on for about 11 s. This circuit is illustrated in Figure 8–28.
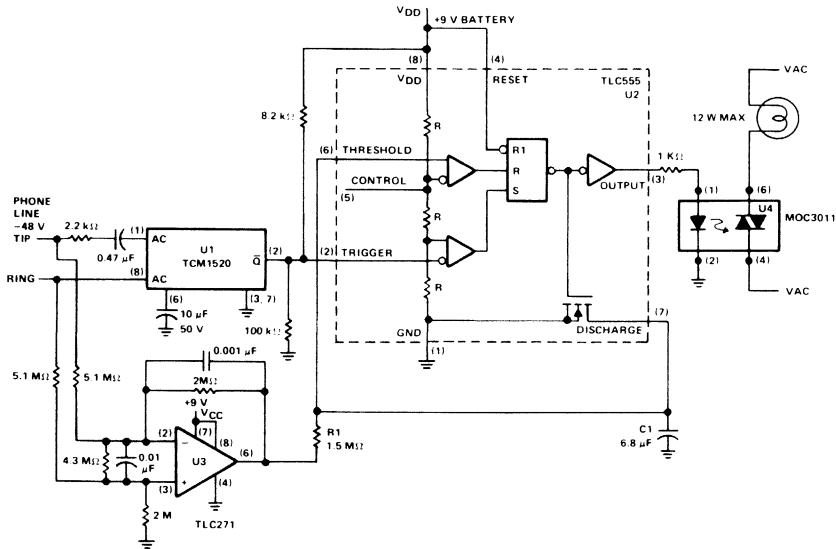
Fig. 8–28   Telephone Controlled Night Light.

Operationally the circuit may be divided into four sections.

1. U1 – TCM1520 Ring Detector

2. U2 – TLC555 Timer

3. U3 – TLC271 End-of-Call Detector

4. U4 – MOC3011 Light Switch

During standby conditions, the −48 V dc bias on the phone line maintains the output of U3 in a high state. Also the timer discharge transistor is on, preventing the charging of timer capacitor C1. When the ac ring signal is applied to the phone line, it is processed by the ring detector U1, producing a negative output pulse at pin 2 for each ring. These pulses are applied to the trigger input (pin 2 of U2) and trigger U2 causing its output to go high and the discharge transistor to turn off. The high output of U2 activates opto-isolator U4 which turns on the night light. The discharge transistor, being off, allows C1 to begin charging.

Each ring retriggers the timer and discharges C1 preventing it from reaching 2/3 V_{DD} threshold level. Thus the night light will remain on while the phone is ringing and for about 11 s after the last ring. After 11 s C1 will be charged to the U2 threshold level (2/3V_{DD}) resulting in the U2 output returning to a low level and its discharge output turning on, discharging C1. At this time the lamp will turn off if the phone is not answered.

When the phone is answered, a 1 kΩ load is placed across the phone line (tip and ring in Figure 8–28). This removes the differential input to operational amplifier U3, causing its output to go low and capacitor C1 starts discharging through R1. As long as the voltage across C1 remains low, timer U2 cannot start its cycle and the lamp will remain on.

When the phone is hung up the low impedance is removed from the phone line and the differential voltage across the line causes the U3 output to go high. This allows C1 to start charging, initiating the timing that will turn off the night light.

uA2240 PROGRAMMABLE TIMER/COUNTER

The uA2240 programmable timer/counter is a special class of timer IC. This device includes a timing section made up of a timer similar to a 555 type, an eight-bit counter, a control flip-flop, and a voltage regulator. Timing periods from microseconds to days may be programmed with an accuracy of 0.5%. Two timing circuits cascaded can generate time delays of up to three years. The 2240 may be operated in either the monostable or astable mode with programmable timing in either mode. A functional diagram and pin-out are shown in Figure 8–29.

Definition of uA2240 Functions

Voltage Regulator (V_{REG})

The on-chip regulator provides voltage to the binary counter and control logic and through pin 15 to external circuits. If V_{CC} (pin 16) is 15 V, V_{REG} is typically 6.3 V. For V_{CC} = 5 V, V_{REG} is typically 4.4 V. For a V_{CC} supply of less than or equal to 4.5 V, pin 16 (V_{CC}) should be
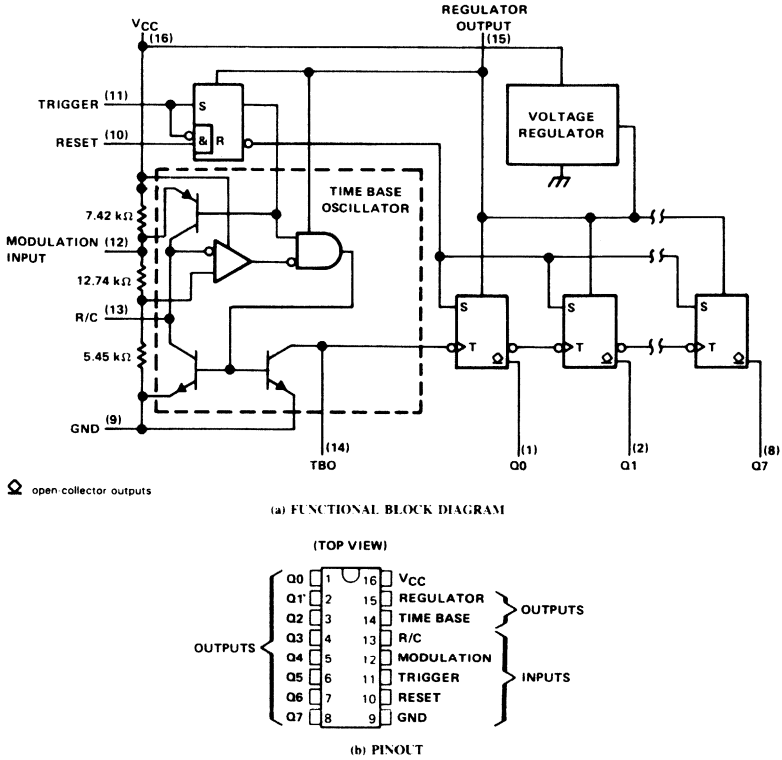
Fig. 8–29   uA2240 Functional Block Diagram and Pinout.

shorted to pin 15 (V_{REG}). The minimum supply voltage for this condition is 4 V. When supplying external circuitry via pin 15 (regulator output), the output current should be 10 mA or less.

Control Logic

The control logic provides trigger and reset signals to the binary counter and time-base generator. Trigger and reset inputs are high impedance and TTL compatible, requiring only about 10 μA of input current. Therefore, they may be controlled by TTL, low level MOS or CMOS logic, and respond to positive input transitions. The reset (pin 10) terminates the timing cycle by returning the counter flip-flops to zero and disabling the time-base oscillator. A logic-high reset stops the timer and sets all outputs high. When powered on, the uA2240 comes

up in the reset state. A trigger input (pin 11) initiates the timing cycle by enabling the time-base oscillator and setting all outputs low. Once triggered, the circuit is immune to further trigger inputs until the timing cycle is completed or a reset signal is applied. However, the trigger takes precedence if both trigger and reset are applied simultaneously.

Time-Base Oscillator

The heart of a uA2240 is its time-base oscillator that is made up of threshold comparators, a flip-flop, discharge and time-base output transistors, RC input, and a modulation and sync input.

RC Input

A resistor and capacitor connected in series between V_{CC} and ground provide an exponential ramp at the RC input (pin 13). The comparator thresholds are designed to detect at levels allowing a 63% charge time (1 RC time interval). Thus, the time-base output (TBO) pulse will have a period $T = 1$ RC. Figure 8–30 shows the recommended range of timing component values. The timing capacitor leakage currents must be low to allow it to charge to the comparator threshold levels with a large value (1 MΩ or greater) timing resistor.
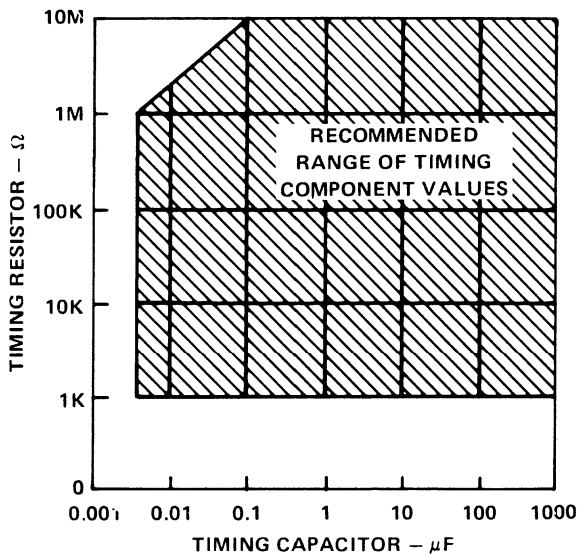
Fig. 8–30   Recommended Range of Timing Component Values.

Modulation and Sync Input

The MOD input (pin 12) is nominally at 71% of the V_{CC} level due to internal biasing. This level may be varied by connecting a resistor from pin 12 to ground or V_{CC}, or by applying an external voltage. This change, or modulation, of voltage on pin 12 changes the upper threshold for the time-base comparator resulting in a change, or modulation, of the time-base period T. Figure 8–31 illustrates the effects of an externally applied modulation voltage on the time-base period.
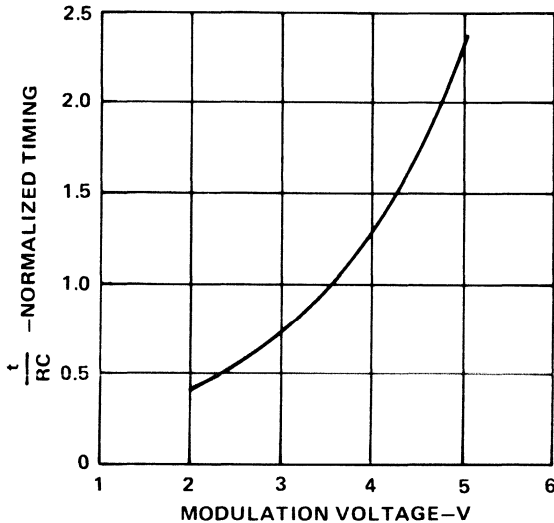
Fig. 8–31   Normalized Change in Time Base Period as a Function of Modulation Voltage at Pin 12.

The MOD input may also be used to synchronize the time-base oscillator with an external clock. Synchronization is achieved by setting the time-base period (T) to be an integer multiple of the sync pulse periods (T_S). This is accomplished by choosing R and C timing components so that:

$$T = RC = T_S \times M$$

where: M is an integer from 1 to 10.

Figure 8–32 gives the typical pull-in range for harmonic synchro-nization versus the ratio of time-base period to sync pulse period (T/T_S).
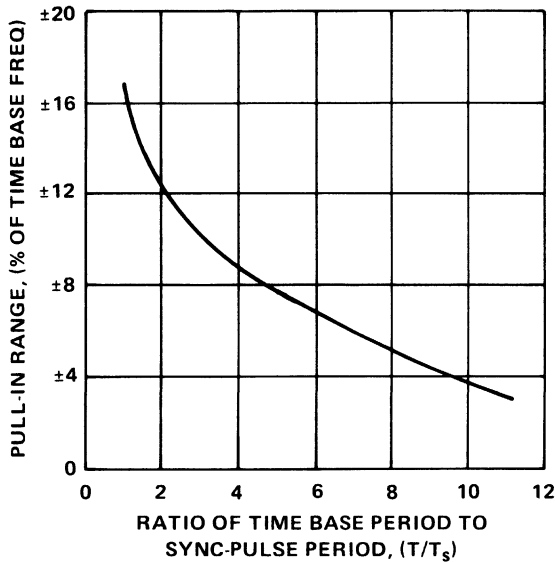
Fig. 8–32   Typical Pull-In Range for Harmonic Synchronization.

Threshold Comparators

The two levels of threshold are set at 21.3% and 71% of V_{CC}. Charging and discharging of the timing capacitor occurs between these two levels. When charging from the 21.3% level toward V_{CC} to the second threshold at 71%, the percentage interval to be changed is (71–21.3) or 49.7%. The actual percentage of the range from 21.3% to the V_{CC} rail is 78.7% so the charge range to be covered is 0.497/0.787 or 63%, exactly one RC time constant. The resulting time base $T = RC$.

Oscillator Flip-flop

Comparator outputs feed the oscillator flip-flop which controls the discharge and time-base output (TBO) transistors. Once triggered (see Figure 8–33) the oscillator continues to run until reset. Output pulses from the TBO are internally connected to the counter input for automatic triggering. The TBO output is an open-collector transistor

and requires a pull-up resistor (typically 20 kΩ) to be connected to the V_{REG} output (pin 15). Grounding the TBO output (pin 14) will disable the counter section.

NOTE: When using a high supply voltage ($V_{CC}>7$ V) and a small timing capacitor ($C<0.1$ µF) the pulse width of the TBO output may be too narrow to trigger the counter section. Connecting a 300 pF capacitor from pin 14 to ground will widen the TBO output pulse width and allow a proper trigger time. This capacitor is also recommended to improve noise immunity.
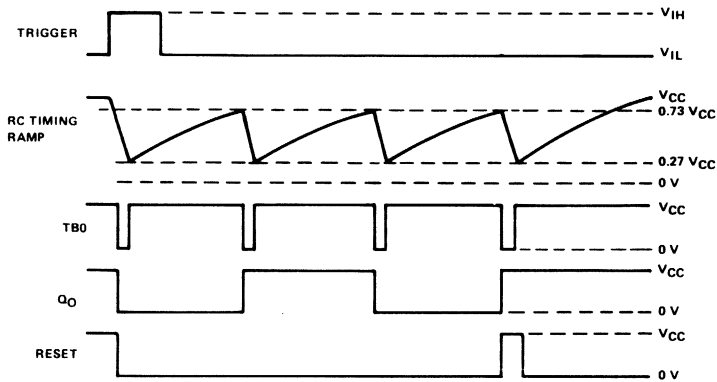
Fig. 8–33   Timing Diagram.

Binary Counter

The uA2240 has an on-chip 8-bit binary counter with outputs that are buffered open-collector type stages. Each output is capable of sinking 2 mA at $V_{OL} = 0.4$ V. At turn on, or in the reset condition, all counter outputs are high, or in the off state. Following a trigger input (Figure 8–34) the outputs will change states according to the sequence shown. The outputs may be used individually, or can be connected together in a wired-OR configuration for special programming.

Combining counter outputs in a wired-OR configuration results in the addition of the time delays associated with each output connected together. As an example pin 5 alone results in a timing cycle (T_O) that is equal to 16T. Similarly connecting Q_0 (pin 1), Q_4 (pin 5), and Q_7 (pin 8) together will yield $T_O = (1 + 16 + 128)T = 145$ T. A proper selection of counter output terminals will allow programming of T_O from 1 to 225 T.
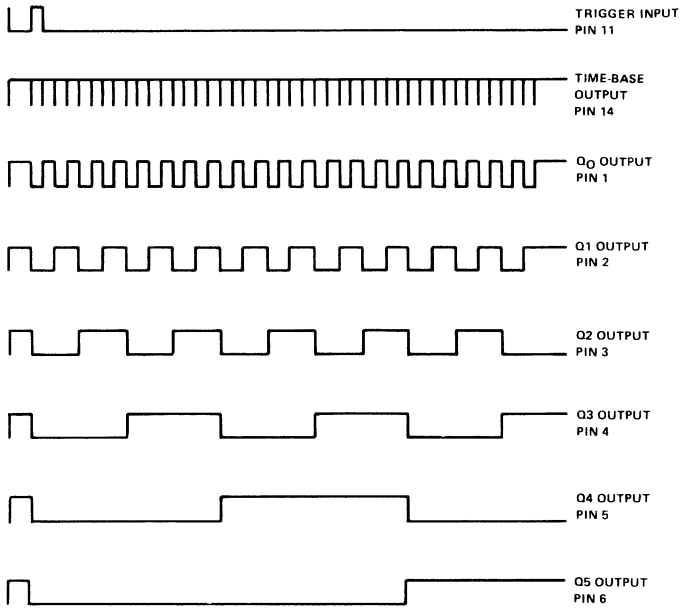
Fig. 8–34   Timing Diagrams of Output Waveforms.
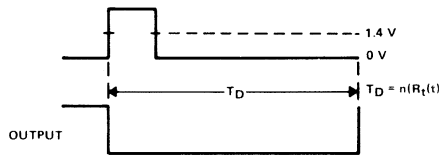
Fig. 8–35   uA2240 Monostable Mode Circuit.

uA2240 Basic Operating Modes

Monostable Operating Mode

Figure 8–35 illustrates the 2240 used in the monostable mode.

In the circuit R_t and C_t set the time base, T, for the desired time period, T_O. Programming of various output times may be accomplished by connecting the desired counter output pins together. The timer output appears across R_L. The output pulse width, T_O, is equal to the number of timing pulses, n, multiplied by R_tC_t or $T_O = nR_tC_t$.

As shown in the timing diagram the output is high (at V_{CC}) prior to triggering. When a trigger pulse is received, the output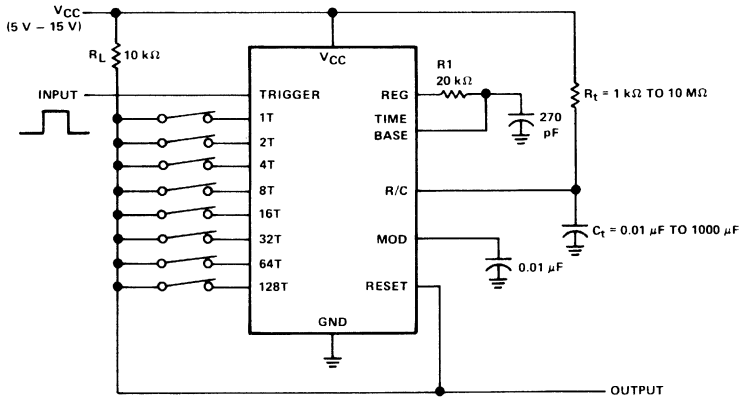 falls low and the timing cycle is initiated. The time-base oscillator will now run until the counter reaches the count programmed by the selector switches or jumpers. When this count is reached, the output rises from the low level to V_{CC}. This rise in level is fed to the reset input, which stops the oscillator and resets the counter. The timer is now in its standby state, awaiting the next trigger pulse.

R1 is a load resistor for the time-base output. The 270 pF capacitor on the time-base pin is a noise bypass to ensure noise immunity within the time-base oscillator. The range of values for Rt and Ct are indicated on the circuit diagram. The maximum oscillator frequency should be limited to about 100 kHz.

Astable Operating Mode

The astable mode circuit is shown in Figure 8–36(a). This circuit is similar to the monostable circuit with the exception that the reset is not connected to the output. This allows the oscillator to continue oscillating once started by a trigger pulse. With a single counter output connected to R_L and the output bus, the frequency of oscillation will be:

$$f_o = \frac{1}{2nR_tC_t}$$

where: n is the counter tap selected (1, 2, 4, 8, etc.).

The factor 2 is required because the basic timing taps are multiples of 1/2 cycle.
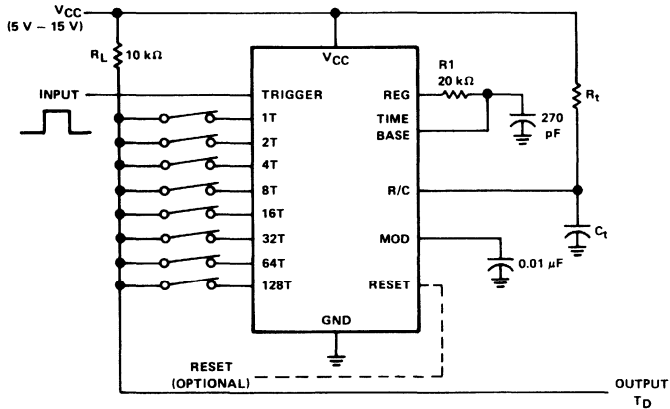
(a) CIRCUIT
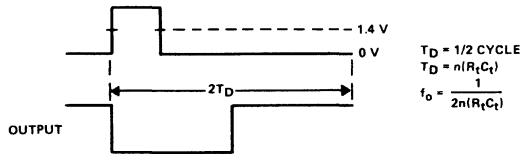
(b) VOLTAGE WAVEFORMS

Fig. 8–36   uA2240 Astable Mode Circuit.

This circuit will not self-start on power-up. A pulse applied to the trigger input will start the synchronous oscillations. The oscillator may be stopped by applying a reset pulse, which causes the output to go high. It will remain in this state until triggered again. If automatic power-up oscillation is desired, connect the trigger input to pin 15 (regulator output). The timing component ranges shown in the monostable circuit, Figure 8–35, are applicable to the astable mode circuit.

Accuracy

The 2240 timer is somewhat more complex than the 555 family. Timing accuracy is good, typically 0.5% for $V_{CC} = 5$ V. The maximum operating frequency is about 130 kHz. The trigger and reset inputs have a threshold sensitivity of 1.4 V.

General Design Considerations

Several precautions should be taken with respect to the V_{CC} supply. The most important is good power supply filtering and bypassing. Ripple on the supply line can cause loss of timing accuracy. A capacitor from V_{CC} to ground, ideally directly across the device, is necessary. The amount of capacitance will depend on the specific application and values from 0.01 μF to 10 μF are not uncommon. The capacitor should be as close to the device as physically possible.

If timing accuracy is to be maintained, stable external components are necesary. Most of the initial timing error is due to the inaccuracies of the external components. The timing resistors should be the metal film type if accuracy and repeatability are important design criteria. If the timing is critical, an adjustable timing resistor is necessary. A good quality multi-turn pot might be used in series with a metal film resistor to make up the R portion of the RC network.

The timing capacitor should also be high quality, with very low leakage. Do not use ceramic disc capacitors in the timing network under any circumstance. Several acceptable capacitor types are silver mica, mylar, polystyrene, and tantulum. If timing accuracy is critical over temperature, timing components with a small positive temperature coefficient should be chosen. The most important characteristic of the capacitor is low leakage. Obviously any leakage will subtract from the charge count causing the actual time to be longer than the calculated value.

One final precaution should be observed. Make certain that the power dissipation of the package is not exceeded. With extremely large timing capacitor values, a maximum duty cycle which allows some cooling time for the discharge transistor may be necessary.

uA2240 APPLICATIONS

Programmable Voltage Controlled Timer

The uA2240 may easily be configured as a programmable voltage controlled timer with a minimum number of external components. The

basic programmable timer circuit is shown in Figure 8–37, including the functional clock diagram of the uA2240. Counter outputs Q2 through Q6 are not shown.

Fig. 8–37 Programmable Voltage Controlled Timer.

A useful feature of the uA2240 timer is the modulation input (pin 12), which allows external adjustment of the input threshold level. A variable voltage is applied to pin 12 from the arm of a 5 KΩ potentiometer connected from V_{CC} to ground. A change in the modulation input voltage will result in a change in the time base oscillator frequency and the period of the time base output (TBO). The time-base period may be trimmed via the modulation input to supply the exact value desired, within the limits determined by the values of R1 and C1. In this application, the basic time-base period set by R1 and C1 is 0.5 ms.

The effect of the voltage modulation input on the time-base oscillator period is shown in Figure 8–38. Although the voltage that can be safely applied to pin 12 may range from V_{CC} to ground, oscillator operation may cease near V_{CC} (within 0.5 V). Note that the chart also shows TBO operation inhibited with modulation inputs below approximately 2 V. With a modulation input voltage of 3.5 V, the Q5 connection gives an active low output for 32 cycles of the time base oscillator, or 16 ms in the case of the circuit shown in Figure 8–37.
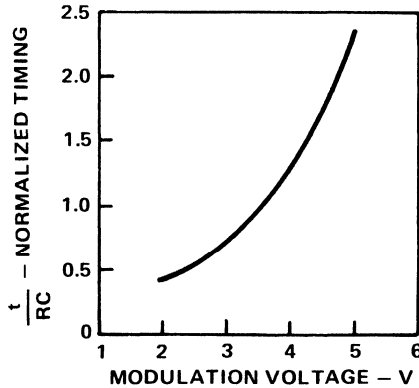
Fig. 8–38   Modulation Voltage Control of Time-Base Period.

The TBO has an open-collector output that is connected to the regulator output via a 20 kΩ pull-up resistor. The output of the TBO drives the input to the 8-stage counter section.

At start-up, a positive trigger pulse starts the TBO and sets all counter outputs to a low state. The trigger pulse duration must be at least 2 μs with a voltage level exceeding 2 V. Once the uA2240 is initially triggered, any further trigger inputs are ignored until it is reset.

The binary outputs are open-collector stages that may be connected together to the 10 kΩ pull-up resistor to provide a 'wired-OR' output function. The combined output is low if any single connected counter output is low. In this application, the output is connected to the reset input through a 47 kΩ resistor.

This circuit may be used to generate 255 discrete time delays that are integer multiples of the time-base period. The total delay is the sum of the number of time-base periods, which is the binary sum of the Q outputs connected. For example, if only Q5 is connected to the reset input, each trigger pulse generates an active-low output for 32 periods of the time-base oscillator. If Q0, Q2 and Q3 are connected together, the binary count is: 1 + 4 + 8 = 13. Thus, 225 discrete time delays are available with the eight counter outputs, Q0 through Q7. Delays from 200 μs to 0.223 s are possible with this configuration.

Frequency Synthesizer

The uA2240 may be easily connected to operate as a programmable voltage controlled frequency synthesizer as shown in Figure 8–39. The uA2240 consists of four basic circuit elements: (1) a time-base oscillator, (2) an eight-bit counter, (3) a control flip-flop, and (4) a voltage regulator.
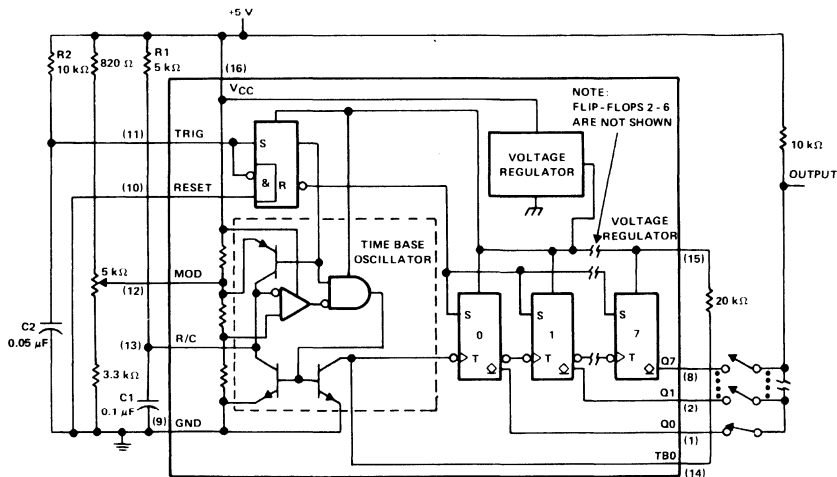

Fig. 8–39   Programmable Voltage Controlled Frequency Synthesizer.

The basic frequency of the time-base oscillator (TBO) is set by the external time constant determined by the values of R1 and C1 ($1/R1C1 = 2$ kHz). The basic frequency may be changed by varying the modulation input voltage supplied to terminal 12. With a modulation voltage range of 2 to 4.5 V, the basic frequency multiplier is changed from 0.4 to 1.75 nominally with $V_{CC} = 5$ V. See Figure 8–38.

The open-collector output of the TBO is connected to the regulator output via a 20 kΩ pull-up resistor, and drives the input to the eight-bit counter. Each counter output is an open-collector stage that may be connected to the 10 kΩ load pull-up resistor to provide a 'wired-OR' function. The combined output is low if any single counter output is low.

At power-up, a positive trigger pulse is detected across C2 which starts the TBO and sets all counter outputs to a low state. Once the uA2240 is initially triggered, any further trigger inputs are ignored until it is reset. In this astable operation, the uA2240 will free-run from the time it is triggered until it receives an external reset signal.

Up to 255 discrete frequencies may be synthesized by connecting different counter outputs. For example, connecting the counter outputs of Q0, Q2, and Q3 supplies the output waveform shown in Figure 8–40 if the modulation voltage is set at 3.5 V, the TBO frequency is 2 kHz, then the output frequency will be 125 Hz. By adjusting the modulation voltage, the TBO frequency may be trimmed from 800 Hz to 3.5 kHz. A wide range of basic time-base frequencies are also available to the designer through the selection of different values of R1 and C1. This includes time-base frequencies as high as 100 kHz. The RC and modulation inputs, pins 12 and 13, have high speed capability and sensitivity for accurate, repeatable performance. It is essential, therefore, that high frequency layout and lead dress techniques be used to avoid noise problems which could result in undesirable jitter on the output pulse.
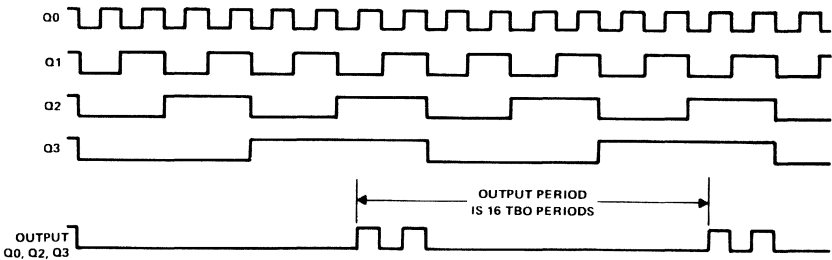

Fig. 8–40   Output Waveform with Q0, Q2, and Q3 Connected.

Cascaded Timers for Long Time Delays

Two uA2240 timers may be cascaded to provide long time delays as shown in Figure 8–41. Each uA2240 counter consists of a time-base oscillator, an eight-bit counter, a control flip-flop, and a voltage regulator. The frequency of the time-base oscillator (TBO) is set by the time constant of an external resistor and capacitor.
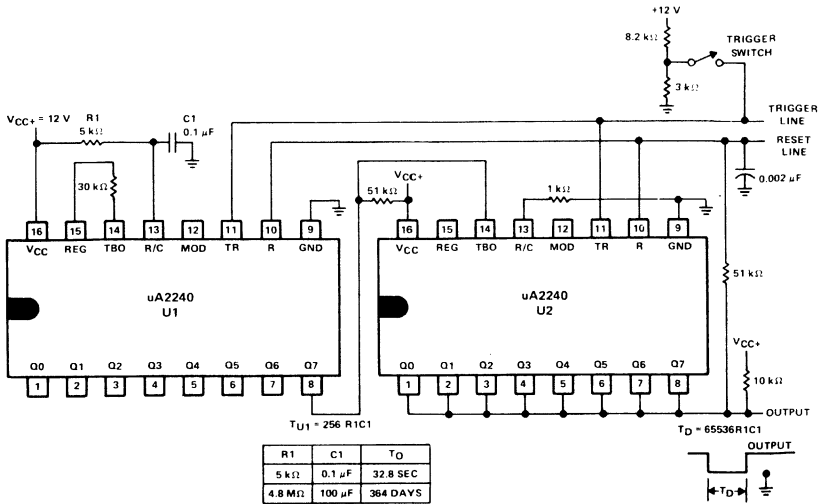
Fig. 8–41   Cascaded Operation for Long Delays.

R1	C1	T₀
5 kΩ	0.1 µF	32.8 SEC
4.8 MΩ	100 µF	364 DAYS

The open-collector output of the TBO drives the internal eight-bit counter if the TBO output is connected to the regulator output via a pull-up resistor. Otherwise, an external source can be connected to the TBO terminal to supply the input to the eight-bit counter. The open-collector counter outputs Q0 through Q7 provide a 'wired-OR' function. The combined output is low if any of the connected counter outputs is low.

The trigger and reset inputs to the internal control flip-flop determine the uA2240 operational state. Once the positive trigger pulse starts the TBO and resets all counter outputs to a low level, further trigger signals are ignored until a reset pulse is received. The reset input inhibits the TBO output and sets all counter outputs to a high level.

In this application, the TBO frequency of U1 is set at 2 kHz by the time constant of R1 and C1. This provides a circuit time-base period of 0.5 ms that drives the internal eight-bit counter of U1.

When the trigger switch is momentarily closed, the trigger input starts the U1 TBO and sets all outputs low. The U1 TBO output is connected to it regulator output through the 30 kΩ pull-up resistor. At the end of 256 U1 time-base periods, the U1 Q7 counter output

generates a negative-going transition that supplies the active time-base (clock) input for U2. This clock input has a period of 128 ms and is active until a reset is generated by a high U2 output. The U2 time-base oscillator is inhibited by connecting its trigger input (pin 13) to ground through a 1 kΩ resistor.

The U2 counter outputs are connected together resulting in a continuous low U2 output until its final count of 256. At this time, all U2 outputs are high. This ends the output pulse period and resets both uA2240 counters. Thus, the output period is low for about 33 s (256 × 128 ms). If the values of R1 and C1 are changed to 4.8 MΩ and 100 μF, respectively, the output period duration will be about 1 year.

uA2240 Operation with External Clock

The uA2240 programmable timer/counter may be operated by an external clock as shown in Figure 8–42. The internal time-base oscillator is disabled by connecting the trigger input (pin 13) to ground through a 1 kΩ resistor. An external clock is applied to the time-base output (TBO), pin 14. For proper operation, the minimum clock amplitude and pulse-duration are 3 V and 1 μs respectively.
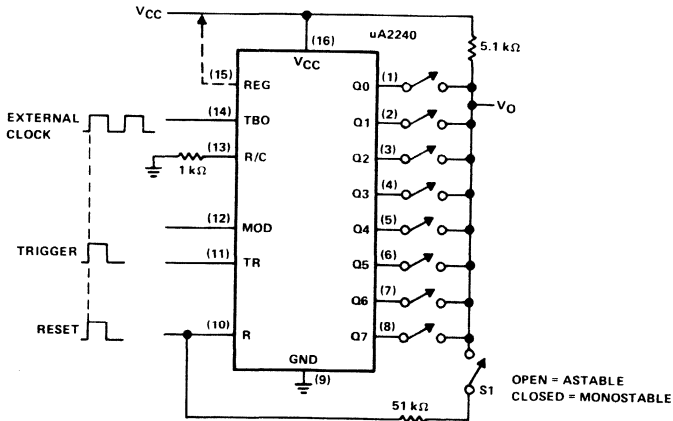

Fig. 8–42   Operation with External Clock.

In this application the uA2240 consists of an eight-bit counter, a control flip-flop, and a voltage regulator. The external clock triggers the

eight-bit counter on the negative-going edge of the clock pulse. The open-collector counter outputs are connected together to the 5.1 kΩ pull-up resistor to provide a 'wired-OR' function where the combined output is low if any one of the outputs is low. This arrangement provides time delays or frequency outputs that have a period equal to integer multiples of the external clock time-base period.

In the astable mode, the uA2240 will free-run from the time it is triggered until it receives an external reset signal. If the monostable mode is selected, one or more of the counter outputs is connected to the reset terminal, and provides the reset at the end of the pulse delay period.

For operation with a supply voltage of 6 V or less, the internal time-base can be powered down by open-circuiting pin 16 and connecting pin 15 to V_{CC}. In this configuration, the internal time-base does not draw any current, and the overall current drain is reduced by approximately 3 mA.

uA2240 Staircase Generator

The uA2240 timer/counter combined with a precision resistor ladder network and an operational amplifier form the staircase generator shown in Figure 8–43. The uA2240 consists of a time-base oscillator, an eight-bit counter, a control flip-flop, and a voltage regulator.
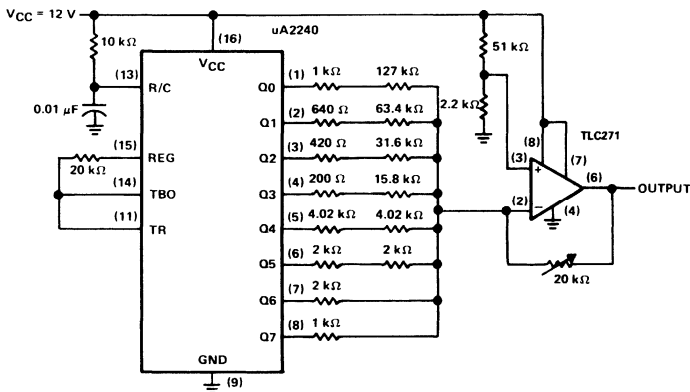

Fig. 8–43   Staricase Generator Circuit.

In the astable mode, once a trigger pulse is applied, the uA2240 operates continuously until it receives a reset pulse. The trigger input (pin 11) is tied to the time base output (pin 14) resulting in automatic starting and continuous operation. The frequency of the time-base oscillator (TBO) is set by the time constant of R1 and C1 (f = 1/R1C1), for this example, a 10 kΩ resistor and 0.01 μF capacitor form the timing network. The total ramp generation time is 25.6 ms for an output frequency of 39.1 Hz. The open-collector TBO output is connected to the regulator output via a 20 kΩ pull-up resistor, and drives the input to the eight-bit counter.

The counter outputs are connected to a precision resistor ladder network with binary weighted resistors. The current sink through the resistors connected to the counter outputs correspond to the count number. For example, the current sink at Q7 (most significant bit) is 128 times the current sink at Q0 (least significant bit).

The positive bias of approximately 0.5 V applied to the non-inverting input of the operational amplifier generates a current feedback at the inverting input that supplies the current sink for the open-collector pull-up resistors. As the count is generated by the uA2240 eight-bit counter, the current sink through each active binary weighted resistor decreases the positive output of the operational amplifier in discrete steps.

The feedback potentiometer is set at a nominal 10 kΩ to supply a maximum output voltage range. A 12 V supply was used to allow a 10 V output swing. Operation from a single 5 V supply will require an adjustment of the gain (feedback resistor) and reference voltage. With a
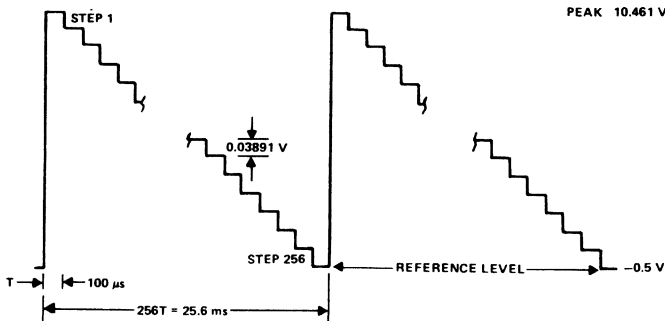

Fig. 8–44   Staircase Generator Voltage Waveforms.

feedback resistance of 4.5 kΩ and a reference of 0.4 V, the output will allow a 3.6 V output change from 0.4 V to 4.0 V in 14.1 mV steps.

The staircase waveform is shown in Figure 8–44. With a 0.5 V input reference on pin 3 of the TLC271, the output will change from 10.46 V maximum, in 256 steps of 38.9 mV per step, to a 0.5 V minimum. Each step has a pulse duration of 100 μs and an amplitude decrease of 38.9 mV. The period of the staircase waveform is 25.6 ms and the waveform output is repeated until a reset is applied to the uA2240.

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